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**2-WIRE REAL-TIME CLOCK**

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**S-35390A**

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The S-35390A is a low-current-consumption 2-wire CMOS real-time clock IC that features a wide operating voltage range (1.3 V to 5.5 V) and can be driven on a variety of supply voltages, from a main supply to a backup supply. The time keeping current consumption of 0.25  $\mu$ A and minimum time keeping operation voltage of 1.1 V enable greatly increased battery duration.

In a system that operates on a backup battery, the free register incorporated in the real-time clock can be used for the user backup memory function. The user register can hold data on a supply voltage as low as 1.2 V (min.), so the data stored in the register before the main power supply was cut can be called any time after the voltage is restored.

This product also includes a clock adjustment function that enables wide-ranging correction of deviation in the frequency of the crystal oscillator at a minimum resolution of 1 ppm. Also, by combining this function with a temperature sensor, the clock adjustment value can be set in accordance with changes in the temperature, which makes it possible to realize a clock function that retains a high degree of accuracy regardless of temperature variation.

**■ Features**

- Low current consumption: 0.25  $\mu$ A typ. ( $V_{DD} = 3.0$  V,  $T_a = 25^\circ\text{C}$ )
- Wide operating voltage range: 1.3 to 5.5 V
- Minimum time keeping operation voltage: 1.1 V
- Built-in clock adjustment function
- Built-in free user register
- 2-wire (I<sup>2</sup>C-BUS)\*1 CPU interface
- Built-in alarm interrupter
- Built-in flag generator at power down or power on
- Auto calendar up to the year 2099, automatic leap year calculation function
- Built-in constant voltage circuit
- Built-in 32 kHz crystal oscillator circuit ( $C_d$  built in,  $C_g$  external)
- Package: 8-pin SOP (JEDEC), 8-pin TSSOP, SNT-8A

\*1. I<sup>2</sup>C-BUS is a trademark of Philips Electronics N.V.

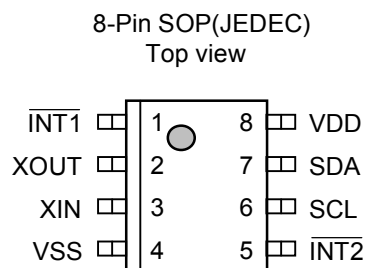
**■ Applications**

- Digital still cameras
- Digital video cameras
- Electronic power meters
- DVD recorders
- TVs, VCRs
- PHS
- Mobile phones
- Car navigation

## ■ Packages

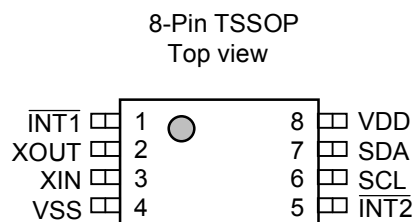
Package Name	Drawing Code		
	Package	Tape	Reel
8-Pin SOP(JEDEC)	FJ008-A	FJ008-D	FJ008-D
8-Pin TSSOP	FT008-A	FT008-E	FT008-E
SNT-8A	PH008-A	PH008-A	PH008-A

## ■ Pin Assignment



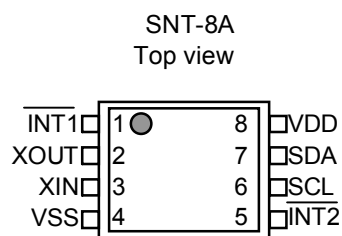
S-35390A-J8T1

**Figure 1**



S-35390A-T8T1

**Figure 2**



S-35390A-I8T1G

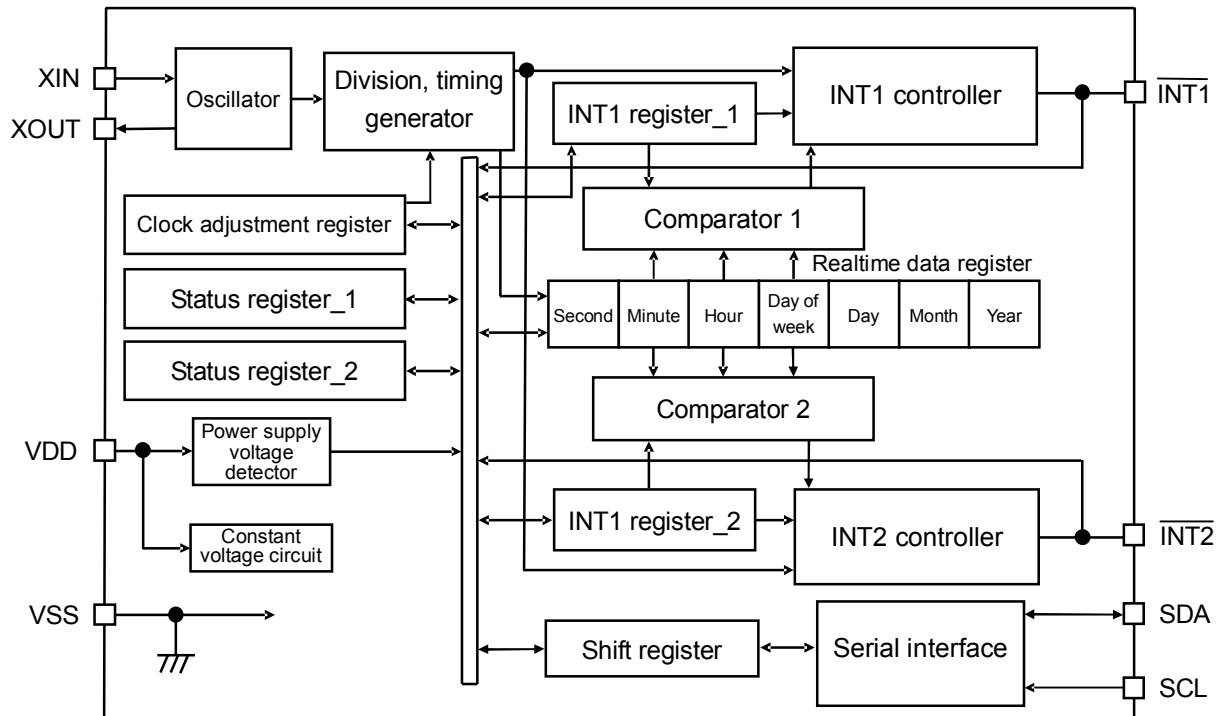
**Figure 3**

## ■ Description of Pins

Table 1

Pin No.	Symbol	Description	Configuration
1	$\overline{\text{INT1}}$	Interrupt 1 signal output pin Depending on the mode set by INT1 register_1 and the status register, it outputs low or a clock when the time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
2	XOUT	Crystal oscillator connect pin (32,768 Hz) (C <sub>d</sub> built in, C <sub>g</sub> external)	
3	XIN		
4	VSS	Negative power supply pin (GND)	
5	$\overline{\text{INT2}}$	Interrupt 2 signal output pin Depending on the mode set by INT1 register_2 and the status register, it outputs low or clock when time is reached. It is disabled by rewriting the status register.	Nch open-drain output (no protective diode on the side of VDD)
6	SCL	Serial clock input pin Since signal processing is done on the SCL signal rising/falling edge, give great care to the rising/falling time and comply strictly with the specifications.	CMOS input (no protective diode on the side of VDD)
7	SDA	Serial data I/O pin Normally, it is pulled up to the V <sub>DD</sub> voltage by a resistor and connected with another open-drain output or open-collector output device via a wired-OR connection.	Nch open-drain output (no protective diode on the side of VDD) CMOS input
8	VDD	Positive power supply pin	

■ **Block Diagram**



**Figure 4**

## ■ Absolute Maximum Ratings

Table 2

Parameter	Symbol	Applicable Pin	Rating	Unit
Power supply voltage	$V_{DD}$		$V_{SS}$ 0.3 to $V_{SS} - 6.5$	V
Input voltage	$V_{IN}$	SCL, SDA	$V_{SS}$ 0.3 to $V_{SS} - 6.5$	V
Output voltage	$V_{OUT}$	SDA, $\overline{INT1}$ , $\overline{INT2}$	$V_{SS}$ 0.3 to $V_{SS} - 6.5$	V
Operating temperature	$T_{opr}$		40 to +85	°C
Storage temperature	$T_{stg}$		55 to +125	°C

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Recommended Operating Conditions

Table 3

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	$V_{DD}$	$T_a = 40$ to $85^{\circ}\text{C}$	1.3	3.0	5.5	V
Operating temperature	$T_{opr}$	$V_{DD} = 1.3$ to $5.5$ V	40	-25	-85	°C
Time keeping voltage range	$V_{DDT}$	$T_a = 40$ to $85^{\circ}\text{C}$	$V_{DDTm}$		5.5	V
Register hold voltage	$V_{DH}$	$T_a = 40$ to $-85^{\circ}\text{C}$	$V_{DDTm}$		5.5	V
Minimum time keeping voltage range	$V_{DDTm}$	$T_a = 40$ to $-85^{\circ}\text{C}$	0.5 <sup>*1</sup>	—	1.1	V
Crystal oscillator $C_L$ value	$C_L$				7.0	pF

\*1. Reference value

## ■ Oscillation Characteristics

Table 4

( $T_a = 25^{\circ}\text{C}$ ,  $V_{DD} = 3.0$  V, DS-VT-200 crystal oscillator ( $C_L = 6$  pF, 32,768 Hz) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Oscillation start voltage	$V_{STA}$	Within 10 seconds	1.1		5.5	V
Oscillation start time	$t_{STA}$	$V_{DD} = 3.0$ V			1	s
IC-to-IC frequency deviation <sup>*1</sup>	$\Delta f/f$		10		+10	ppm
Frequency voltage deviation	$\Delta f/V$	$V_{DD} = 1.3$ to $5.5$ V	3	—	-3	ppm/V
Internal oscillation capacitance (1)	$C_g$	Applied to XIN pin	0		9.1	pF
Internal oscillation capacitance (2)	$C_d$	Applied to XOUT pin	—	8		pF

\*1. Reference value

## ■ DC Electrical Characteristics

**Table 5 DC Characteristics (V<sub>DD</sub> = 3.0 V)**

(Ta = 40 to 85°C, V<sub>DD</sub> = 3.0 V, DS-VT-200 crystal oscillator (C<sub>L</sub> = 6 pF, 32,768 Hz, C<sub>g</sub> = 9.1 pF) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I <sub>DD1</sub>		Out of communication		0.25	0.93	μA
Current consumption 2	I <sub>DD2</sub>		During communication (SCL = 100 kHz)		6	14	μA
Input current leakage 1	I <sub>IZH</sub>	SCL, SDA	V <sub>IN</sub> = V <sub>DD</sub>	0.5		0.5	μA
Input current leakage 2	I <sub>IZL</sub>	SCL, SDA	V <sub>IN</sub> = V <sub>SS</sub>	0.5		0.5	μA
Output current leakage 1	I <sub>OZH</sub>	INT1, INT2, SDA	V <sub>OUT</sub> = V <sub>DD</sub>	0.5		0.5	μA
Output current leakage 2	I <sub>OZL</sub>	INT1, INT2, SDA	V <sub>OUT</sub> = V <sub>SS</sub>	0.5		0.5	μA
Input voltage 1	V <sub>IH</sub>	SCL, SDA		0.8 × V <sub>DD</sub>			V
Input voltage 2	V <sub>IL</sub>	SCL, SDA				0.2 × V <sub>DD</sub>	V
Output current 1	I <sub>OL1</sub>	INT1, INT2	V <sub>OUT</sub> = 0.4 V	3.0	5.0		mA
Output current 2	I <sub>OL2</sub>	SDA	V <sub>OUT</sub> = 0.4 V	5	10		mA
Power supply voltage detection voltage *1	V <sub>DET</sub>		Ta = 40 to 85°C	V <sub>DDTm</sub> - 0.15 *2		V <sub>DDTm</sub> - 0.4	V

\*1. Power supply voltage detection voltage: Constantly maintains the relation of V<sub>DET</sub> > V<sub>DDTm</sub> (minimum time keeping voltage). Refer to **Characteristics**.

\*2. Reference value

**Table 6 DC Characteristics (V<sub>DD</sub> = 5.0 V)**

(Ta = 40 to -85°C, V<sub>DD</sub> = 5.0 V, DS-VT-200 crystal oscillator (C<sub>L</sub> = 6 pF, 32,768 Hz, C<sub>g</sub> = 9.1 pF) manufactured by Seiko Instruments Inc.)

Parameter	Symbol	Applicable Pin	Conditions	Min.	Typ.	Max.	Unit
Current consumption 1	I <sub>DD1</sub>		Out of communication		0.3	1.1	μA
Current consumption 2	I <sub>DD2</sub>		During communication (SCL = 100 kHz)		14	30	μA
Input current leakage 1	I <sub>IZH</sub>	SCL, SDA	V <sub>IN</sub> = V <sub>DD</sub>	0.5		0.5	μA
Input current leakage 2	I <sub>IZL</sub>	SCL, SDA	V <sub>IN</sub> = V <sub>SS</sub>	0.5		0.5	μA
Output current leakage 1	I <sub>OZH</sub>	INT1, INT2, SDA	V <sub>OUT</sub> = V <sub>DD</sub>	0.5		0.5	μA
Output current leakage 2	I <sub>OZL</sub>	INT1, INT2, SDA	V <sub>OUT</sub> = V <sub>SS</sub>	0.5		0.5	μA
Input voltage 1	V <sub>IH</sub>	SCL, SDA		0.8 × V <sub>DD</sub>			V
Input voltage 2	V <sub>IL</sub>	SCL, SDA				0.2 × V <sub>DD</sub>	V
Output current 1	I <sub>OL1</sub>	INT1, INT2	V <sub>OUT</sub> = 0.4 V	3.0	8.0		mA
Output current 2	I <sub>OL2</sub>	SDA	V <sub>OUT</sub> = 0.4 V	6	13		mA
Power supply voltage detection voltage *1	V <sub>DET</sub>		Ta = 40 to 85°C	V <sub>DDTm</sub> - 0.15 *2		V <sub>DDTm</sub> - 0.4	V

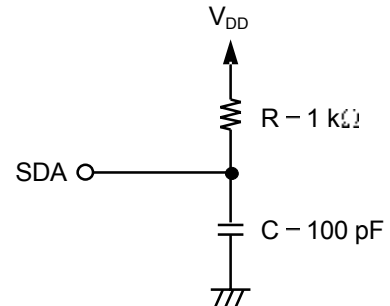
\*1. Power supply voltage detection voltage: Constantly maintains the relation of V<sub>DET</sub> > V<sub>DDTm</sub> (minimum time keeping voltage). Refer to **Characteristics**.

\*2. Reference value

## ■ AC Electrical Characteristics

**Table 7 Measurement Conditions**

Input pulse voltage	$0.1 \times V_{DD}$ to $0.9 \times V_{DD}$
Input pulse rise/fall time	20 ns
Output determination voltage	$0.5 \times V_{DD}$
Output load	100 pF – pull-up resistor 1 k $\Omega$



**Remark** The power supplies of the IC and load have the same electrical potential.

**Figure 5 Output Load Circuit**

**Table 8 AC Characteristics**

(Ta = 40 to –85°C)

Parameter	Symbol	V <sub>DD</sub> = 1.3 to 5.5 V			V <sub>DD</sub> = 3.0 to 5.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f <sub>SCL</sub>	0		100	0		400	kHz
SCL clock “L” time	t <sub>LOW</sub>	4.7			1			μs
SCL clock “H” time	t <sub>HIGH</sub>	4			0.9			μs
SDA output delay time *1	t <sub>PD</sub>	—	—	3.5	—		0.9	μs
Start condition setup time	t <sub>SU. STA</sub>	4.7			0.6			μs
Start condition hold time	t <sub>HD. STA</sub>	4			0.6			μs
Data input setup time	t <sub>SU. DAT</sub>	250			100			ns
Data input hold time	t <sub>HD. DAT</sub>	0			0			ns
Stop condition setup time	t <sub>SU. STO</sub>	4.7						μs
SCL and SDA rise time	t <sub>R</sub>			1			0.3	μs
SCL and SDA fall time	t <sub>F</sub>	—	—	0.3	—		0.3	μs
Bus release time	t <sub>BUF</sub>	4.7			1.3			μs
Noise suppression time	t <sub>I</sub>			100			50	ns

\*1. Since the output format of the SDA pin is Nch open-drain output, the SDA output delay time is determined by the values of the load resistance (R<sub>L</sub>) and load capacity (C<sub>L</sub>) outside the IC. Therefore, use this value only as a reference value.

## ■ Timing Chart

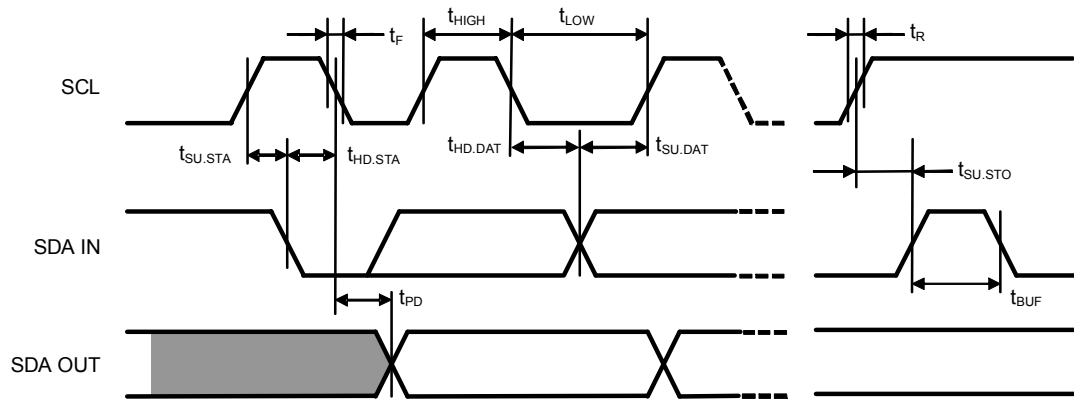


Figure 6 Bus Timing

## ■ Operation

### 1. Communication data configuration

The master device on the system generates a start condition to the slave device to communicate. Then it transmits a 4-bit device address, 3-bit command, and 1-bit read/write command on the SDA bus.

The higher 4 bits that indicate the device address are called the device code and are fixed to "0110". Refer to "Serial Interface".

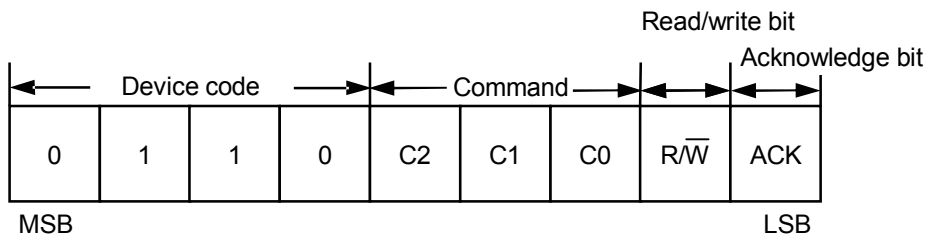


Figure 7 Communication Data



## 2. Command configuration

There are eight types of commands that read from and write to various registers. The table below lists these commands.

**Table 9 Command List**

Command				Data							
C2	C1	C0	Description	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	Status register_1 access	POC <sup>*4</sup>	BLD <sup>*4</sup>	INT2 <sup>*3</sup>	INT1 <sup>*3</sup>	SC1 <sup>*2</sup>	SC0 <sup>*2</sup>	12/24	RESET <sup>*1</sup>
0	0	1	Status register_2 access	TEST <sup>*5</sup>	INT2AE	INT2ME	INT2FE	32kE	INT1AE	INT1ME	INT1FE
0	1	0	Real-time data 1 access (year data to)	Y80 <sup>*6</sup>	Y40 <sup>*6</sup>	Y20 <sup>*6</sup>	Y10 M10	Y8 M8	Y4 M4	Y2 M2	Y1 M1
				<sup>*6</sup>	<sup>*6</sup>	D20	D10	D8	D4	D2	D1
				<sup>*6</sup>	<sup>*6</sup>	— <sup>*6</sup>	<sup>*6</sup>	<sup>*6</sup>	W4	W2	W1
				<sup>*6</sup>	AM/PM	H20	H10	H8	H4	H2	H1
				<sup>*6</sup>	m40	m20	m10	m8	m4	m2	m1
				<sup>*6</sup>	s40	s20	s10	s8	s4	s2	s1
0	1	1	Real-time data 2 access (hour data to)	<sup>*6</sup>	AM/PM	H20	H10	H8	H4	H2	H1
				<sup>*6</sup>	m40	m20	m10	m8	m4	m2	m1
				<sup>*6</sup>	s40	s20	s10	s8	s4	s2	s1
1	0	0	INT1 register_1 access (alarm time 1)	A1WE	<sup>*6</sup>	— <sup>*6</sup>	<sup>*6</sup>	<sup>*6</sup>	W4	W2	W1
			(INT1AE = 1, INT1ME = 0, INT1FE = 0)	A1HE	AM/PM	H20	H10	H8	H4	H2	H1
				A1mE	m40	m20	m10	m8	m4	m2	m1
1	0	1	INT1 register_1 access (frequency duty setting)	SC <sup>*7</sup>	SC <sup>*7</sup>	SC <sup>*7</sup>	16 Hz	8 Hz	4 Hz	2 Hz	1 Hz
			(INT1ME = 0, INT1FE = 1)								
1	0	1	INT1 register_2 access (alarm time 2)	A2WE	<sup>*6</sup>	<sup>*6</sup>	<sup>*6</sup>	<sup>*6</sup>	W4	W2	W1
			(INT2AE = 1, INT2ME = 0, INT2FE = 0)	A2HE	AM/PM	H20	H10	H8	H4	H2	H1
				A2mE	m40	m20	m10	m8	m4	m2	m1
1	1	1	INT1 register_2 access (frequency duty setting)	SC <sup>*7</sup>	SC <sup>*7</sup>	SC <sup>*7</sup>	16 Hz	8 Hz	4 Hz	2 Hz	1 Hz
			(INT2ME = 0, INT2FE = 1)								
1	1	0	Clock adjustment register access	V7	V6	V5	V4	V3	V2	V1	V0
1	1	1	Free register access	F7	F6	F5	F4	F3	F2	F1	F0

\*1. Write-only flag. By writing "1" to this register, the IC is reset.

\*2. Scratch bit. R/W-enabled register that can be freely used by users.

\*3. Read-only flag. It is cleared when read. It is valid only when the alarm is set.

\*4. Read-only flag. "POC" is set to "1" when power is applied. It is cleared when read. For the "BLD", refer to "Power Supply Voltage Detector".

\*5. For IC testing. Normally set this register to "0".

\*6. No effect by writing. It is "0" when read.

\*7. This is a R/W-enabled register that does not affect interrupts.

## ■ Register Configuration

### 1. Real-time data register

The real-time data register is a 56-bit register that stores the BCD code of the year, month, day, day of week, hour, minute, and second data. Any read/write operation performed by the real-time data access command transmits or receives the data from the LSB which is the first digit of the year.

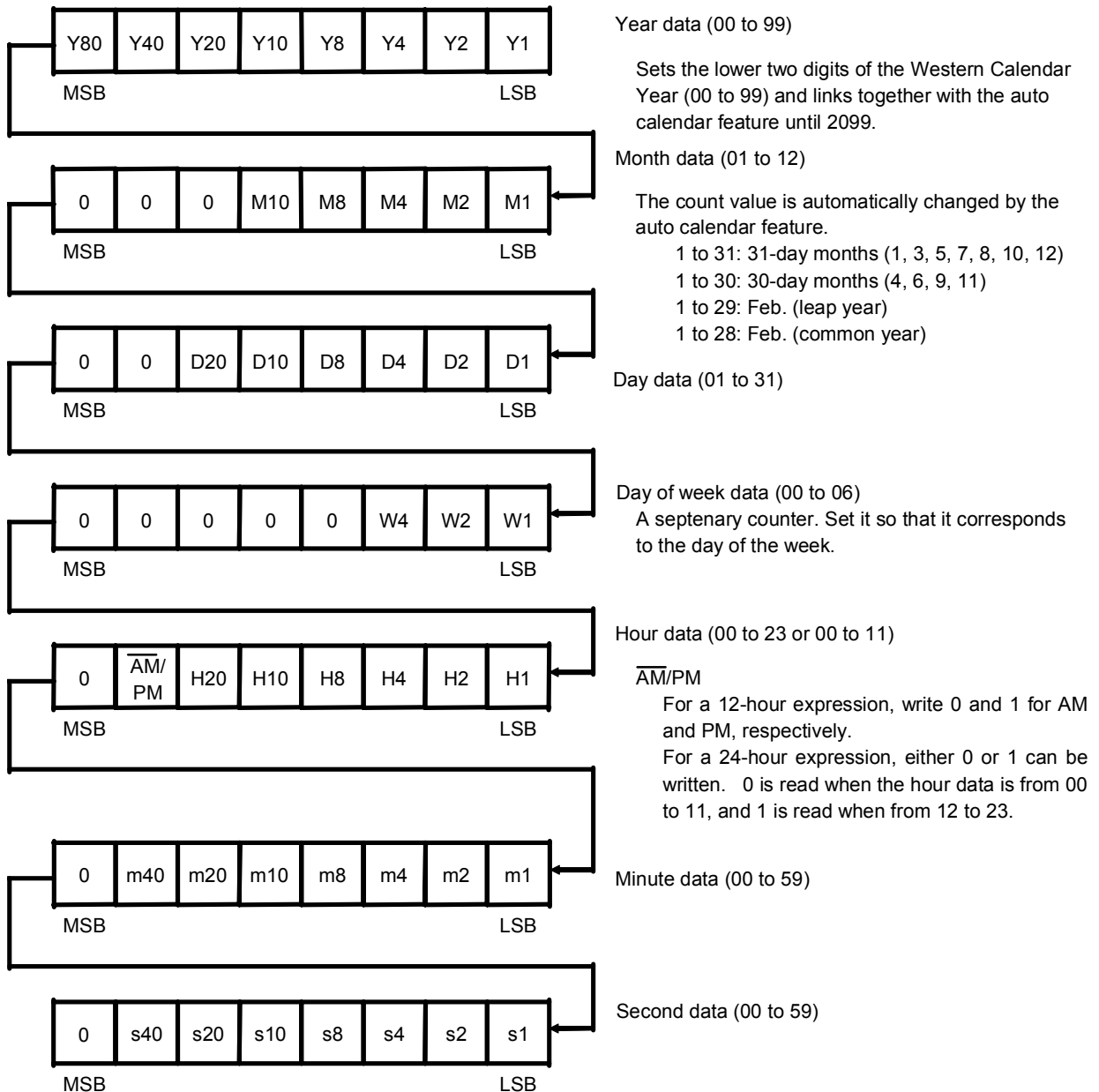
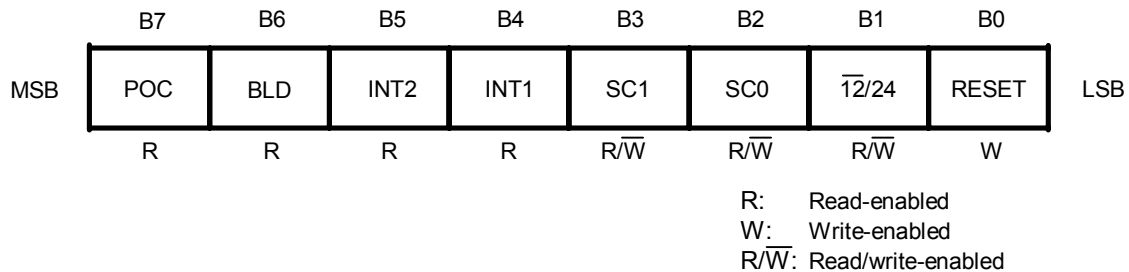


Figure 8 Real-time Data Register

## 2. Status register\_1

Status register\_1 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.

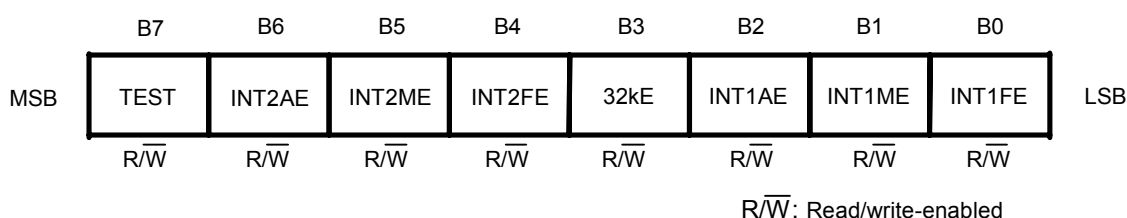


**Figure 9 Status Register\_1**

- B7: POC** This flag is set to “1” at power-on. Once this flag is set to “1”, it is not set to “0” even when the power supply voltage reaches or exceeds the detection voltage ( $V_{DET}$ ). This flag is read-only and can be read by the status register\_1 access command. Once it is read, it is automatically set to “0”. When the flag is “1”, it must be initialized. For the method of initialization, refer to “**Initialization at Power-on and Power-on Detector**”.
- B6: BLD** If the power supply voltage detector detects a voltage of detection voltage ( $V_{DET}$ ) or less this flag is set to “1”, which enables the detection of a power supply voltage drop. Once this flag is set to “1”, it is not set to “0” even when the power supply voltage reaches or exceeds the detection voltage ( $V_{DET}$ ). This flag is read-only and can be read by the status register\_1 access command. Once it is read, it is automatically set to “0”. When the flag is “1”, it must be initialized. For the method of initialization, refer to “**Initialization at Power-on and Power-on Detector**”, and for the operation of the power supply voltage detector, refer to “**Power Supply Voltage Detector**”.
- B5, B4: INT2, INT1**
- When the interrupt signal is output from the  $\overline{INT1}$  or  $\overline{INT2}$  pin using the alarm interrupt function, for an interrupt signal output from the  $\overline{INT1}$  pin, the INT1 flag is set to “1”, and for an interrupt signal output from the  $\overline{INT2}$  pin, the INT2 flag is set to “1”.
- B3, B2: SC1, SC0**
- These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 5.5 V).
- B1: 12/24** This flag is used to set 12-hour or 24-hour expression.
- 0: 12-hour expression  
1: 24-hour expression
- B0: RESET** By setting this bit to “1”, the internal IC is initialized. This is a write-only bit and is always “0” when it is read. Be sure to write “1” to the reset flag when applying the power supply voltage to the IC.

### 3. Status Register\_2

Status register\_2 is an 8-bit register that is used to display and set various modes. The bit configuration is shown below.



**Figure 10 Status Register\_2**

**B7: TEST** The TEST flag is a bit for testing the IC. If the TEST flag is set to "1", the IC is switched to the TEST mode. If this flag is "1", it is necessary to initialize it to "0" by setting the reset flag of status register\_1 to "1".

**B6: INT2AE, B5: INT2ME, B4: INT2FE**

These flags are used to select the output mode from the  $\overline{\text{INT2}}$  pin. Mode selections are shown below. When using the alarm 2 function, after setting the alarm interrupt mode, access INT1 register\_2.

**Table 10 Interrupt Modes ( $\overline{\text{INT2}}$ )**

INT2AE	INT2ME	INT2FE	$\overline{\text{INT2}}$ Pin Output Mode
0	0	0	No interrupt
*1	0	1	Selected frequency steady interrupt
*1	1	0	Per-minute edge interrupt
*1	1	1	Per-minute steady interrupt 1 (50% duty)
1	0	0	Alarm interrupt

\*1. Don't care (Both of 0 and 1 are acceptable).

**B3: 32kE, B2: INT1AE, B1: INT1ME, B0: INT1FE**

These flags are used to select the output mode from the  $\overline{\text{INT1}}$  pin. Mode selections are shown below. When using the alarm 1 function, after setting the alarm interrupt mode, access INT1 register\_1.

**Table 11 Interrupt Modes ( $\overline{\text{INT1}}$ )**

32kE	INT1AE	INT1ME	INT1FE	$\overline{\text{INT1}}$ Pin Output Mode
0	0	0	0	No interrupt
1	*1	*1	*1	32 kHz output
0	*1	0	1	Selected frequency steady interrupt
0	*1	1	0	Per-minute edge interrupt
0	0	1	1	Per-minute steady interrupt 1 (50% duty)
0	1	0	0	Alarm interrupt
0	1	1	1	Per-minute steady interrupt 2

\*1. Don't care (Both of 0 and 1 are acceptable).

#### 4. INT1 register\_1 and INT1 register\_2

INT1 register\_1 and INT1 register\_2 are interrupt setting registers that can be set independently. The interrupts are output from the INT1 pin and INT2 pin. The function is switched by using status register\_2.

##### (1) Alarm interrupt

Data set in INT1 register\_1 and INT1 register\_2 is considered as alarm time data. Having the same configuration as the hour and minute registers of the real-time data register, these registers represent hours and minutes with BCD codes. When setting these registers, do not set any nonexistent day. Data to be set must be in accordance with the 12-hour or 24-hour expression that is set in status register\_1.

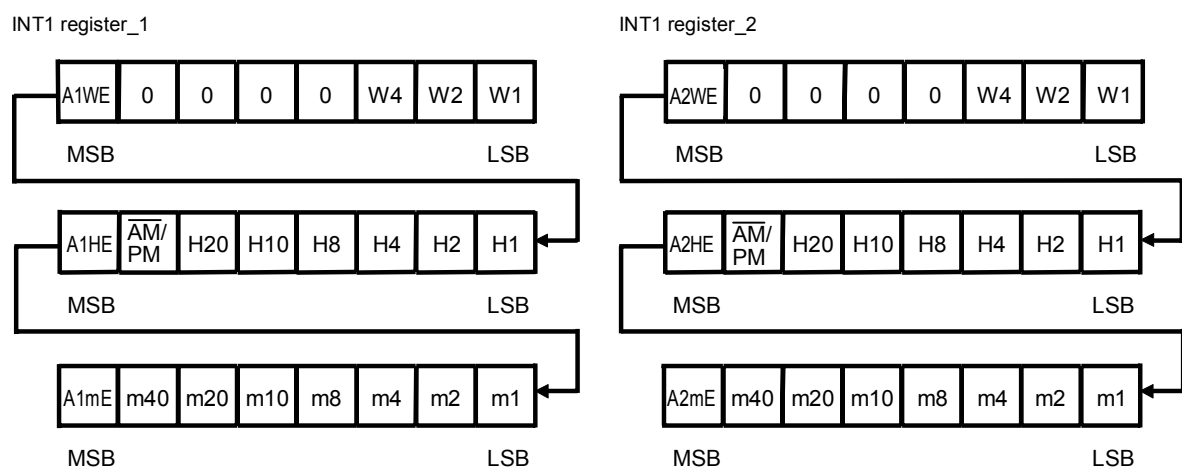


Figure 11 INT1 Register\_1, INT1 Register\_2 (Alarm Time Data)

In INT1 register\_1, A1WE, A1HE, and A1mE are respectively in the MSB of each byte. By setting each bit to "1", the setting of the day of week data, hour data, and minute data in the corresponding byte becomes valid. A2WE, A2HE, and A2mE of INT1 register\_2 are the same.

**The example of setting** In case of the setting alarm time "PM 7:00" in INT1 register\_1

##### (1) 12-hour expression (status register\_1 B1 = 0)

: set up 7:00 PM

Writing in INT1 register\_1

Day of week data	0	*1	*1	*1	*1	*1	*1
Hour data	1	1	0	0	0	1	1
Minute data	1	0	0	0	0	0	0
	MSB						LSB

\*1. Don't care (Both of 0 and 1 are acceptable).

##### (2) 24-hour expression (status register\_1 B1 = 1)

: set up 19:00 PM

Writing in INT1 register\_1

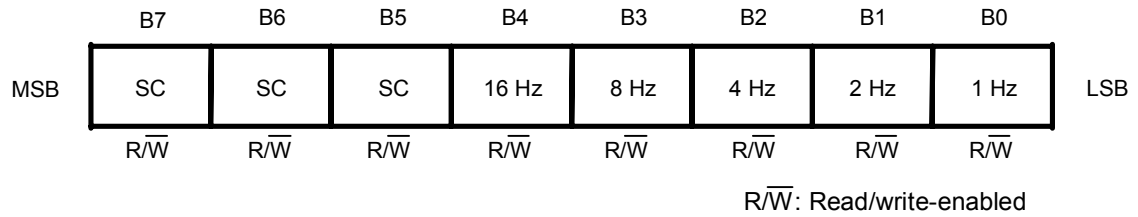
Day of week data	0	*1	*1	*1	*1	*1	*1
Hour data	1	1*2	0	1	1	0	1
Minute data	1	0	0	0	0	0	0
	MSB						LSB

\*1. Don't care (Both of 0 and 1 are acceptable).

\*2. Set up AM/PM flag along with the time setting.

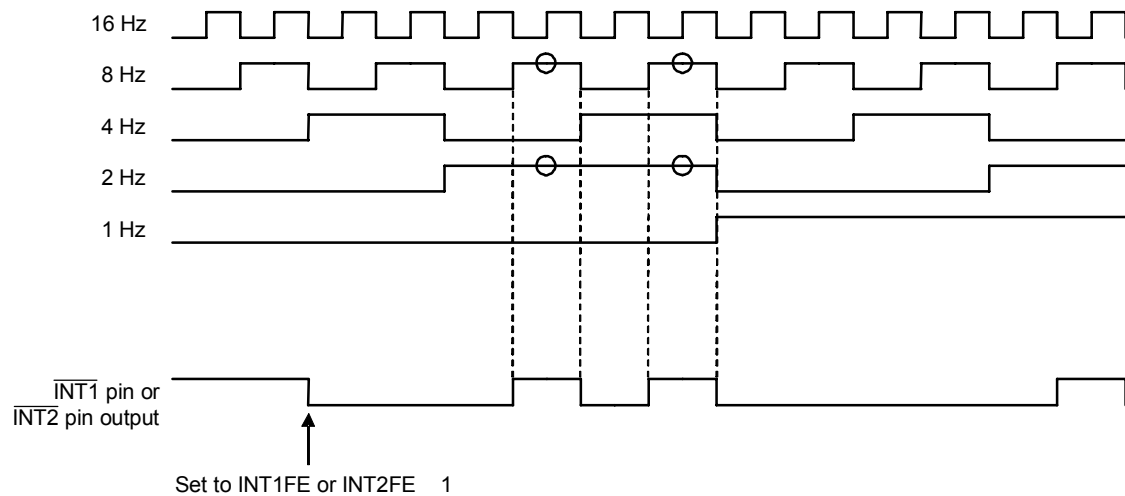
**(2) Selected frequency steady interrupt**

Data set in INT1 register\_1 and INT1 register\_2 is considered as frequency duty data. By setting each bit from B4 to B0 of the register to "1", the frequency corresponding to each bit is selected in an ANDed form. The SC bits configure a 3-bit SRAM type register that can be set freely by users. These bits can be read and written within the operating voltage range (1.3 to 5.5 V). There is no impact on the duty function.



**Figure 12 INT1 Register\_1 and INT1 Register\_2 (Frequency Duty Data)**

**Example**    B4 to B0    0Ah

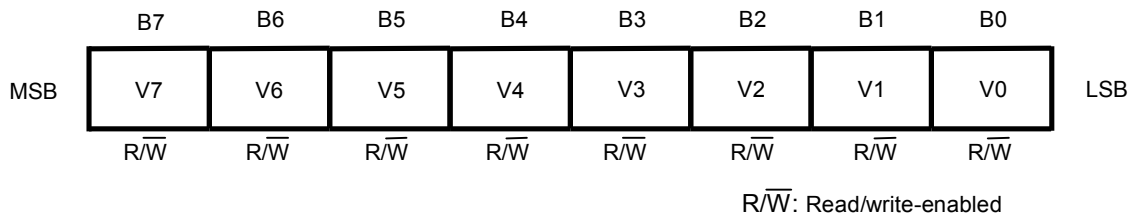


**Figure 13 INT1 Register\_1 and INT1 Register\_2 (Frequency Duty Data) Output Example**

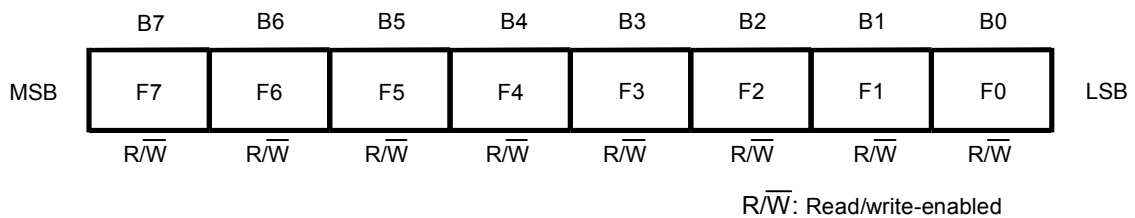
**5. Clock adjustment register**

The clock adjustment register is a 1-byte register that is used to logically correct real-time data. When not using the clock adjustment register, set this register to 00h using the clock adjustment register write command.

For the “register value”, refer to “**Clock Adjustment Function**”.

**Figure 14 Clock Adjustment Register****6. Free register**

The free register is a 1-byte SRAM type register that can be set freely by users. It can be read and written within the operating voltage range (1.3 to 5.5 V).

**Figure 15 Free Register**

## ■ Initialization at Power-on and Power-on Detector

When power is applied to this IC, status register\_1 is set to "80h" (bit 7 (POC flag) of status register\_1 is set to "1") by the power-on detector and a 1 Hz clock is output from the  $\overline{\text{INT1}}$  pin. This function is provided to adjust the oscillation frequency. In normal use, the IC must be initialized at power-on. Initialization is performed by writing "1" to bit 0 (RESET flag) of status register\_1.

Also, the IC must be initialized when the POC flag is set to "1". After initialization, the POC flag is set to "0". For normal operation of the power-on detector, first hold the IC power supply voltage at 0 V and then increase it.

## Register State After Initialization

The state of each register after initialization is as follows.

Real-time data register:	00 (year), 01 (month), 01 (day), 0 (day of week), 00 (hour), 00 (minute), 00 (second)
Status register_1:	"0 0 0 0 B3 B2 B1 0 b" (The B3, B2, and B1 data of status register_1 after initialization are set in B3, B2, and B1.)
Status register_2:	"00h"
INT1 register_1:	"00h"
INT1 register_2:	"00h"
Clock adjustment register:	"00h"
Free register:	"00h"



## ■ Power Supply Voltage Detector

S-35390A has an internal power supply voltage detector, which monitors drops in the power supply voltage by reading the BLD flag. This circuit samples the voltage for only 15.6 ms per second. If the power supply voltage drops below the detection voltage ( $V_{DET}$ ), the BLD latch circuit latches the "H" level, bit 6 (BLD flag) of internal status register\_1 is set to "1", and sampling stops. Detection voltage and release voltage have approximate 0.15 V (Typ.) of hysteresis width respectively (Refer to "Characteristics"). Once "1" is detected in the BLD flag, no detection operation is performed unless initialization is performed or the BLD flag is read by the status register\_1 access command, and "1" is held in the BLD flag. Sampling resumes only when the subsequent communication action is initialization or BLD flag read.

In addition, if this BLD flag is "1" after the power supply voltage is recovered, it must be initialized.

**Caution** In case the power supply voltage falls and returns after the latch circuit latches "H", the BLD flag can be read as "1" by a status register\_1 access command first. After that the sampling is resumed and the read-out of the next BLD flag is performed, the BLD flag is reset and read as "0". Refer to the timing chart below.

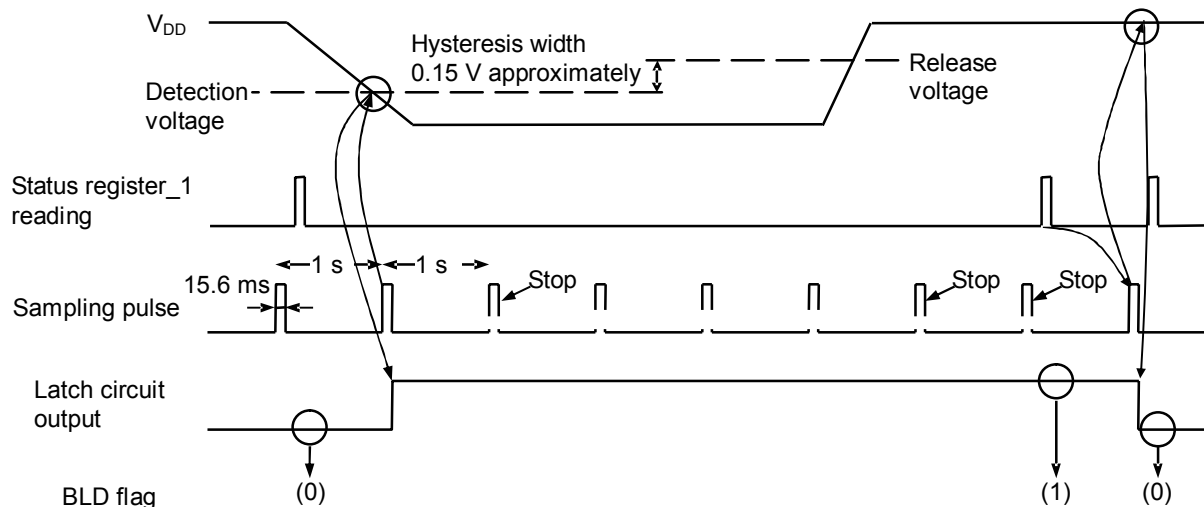


Figure 16 Timing of Power Supply Voltage Detector

## ■ Processing of Nonexistent Data and End-of-Month

When real-time data is written, the data is checked for validity, invalid data is processed, and the end-of-month is corrected.

### 1. Processing of nonexistent data

**Table 12 Processing of Nonexistent Data**

Register	Normal Data	Error Data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data <sup>*1</sup> (24-hour)	0 to 23	24 to 29, 3X, XA to XF	00
	(12-hour) 0 to 11	12 to 19, 2X, 3X, XA to XF	00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data <sup>*2</sup>	00 to 59	60 to 79, XA to XF	00

**\*1.** For 12-hour expression, write the AM/PM flag.

The AM/PM flag is ignored in 24-hour expression, but "0" for 0 to 11 hours and "1" for 12 to 23 hours are read in a read operation.

**\*2.** Processing of nonexistent data for second data is performed by a carry pulse one second after the end of writing. At this point, the carry pulse is sent to the minute counter.

### 2. Processing of end-of-month

A nonexistent day is set to the first day of the next month. If February 30th is written, March 1st is set. Leap year correction is also performed at this time.

## ■ Interrupts

The  $\overline{\text{INT1}}$  pin output mode is selected by the INT1AE, INT1ME, and INT1FE flags of status register\_2. Similarly, the  $\overline{\text{INT2}}$  pin output mode is selected by the INT2AE, INT2ME, and INT2FE flags of status register\_2.

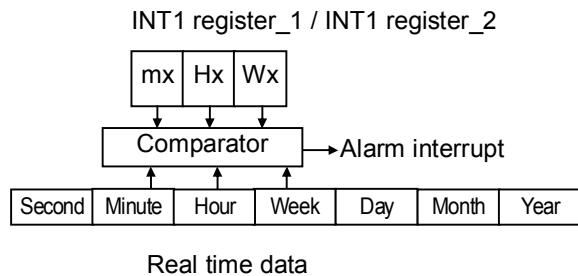
### (1) Alarm interrupt output

When the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin output mode is set as the alarm setting using status register\_2 and the day of week, hour, and minute data is set in INT1 register\_1 (or INT1 register\_2), low is output from the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin when the set hour is reached. Since the output is held, rewrite INT1AE of status register\_2 to "0" (or INT2AE to "0") using serial communication to set the output to high (OFF state).

32kE = 0, INT1ME = INT1FE = 0  
( $\overline{\text{INT1}}$  pin output mode)  
INT2ME = INT2FE = 0  
( $\overline{\text{INT2}}$  pin output mode)

Alarm enable flag

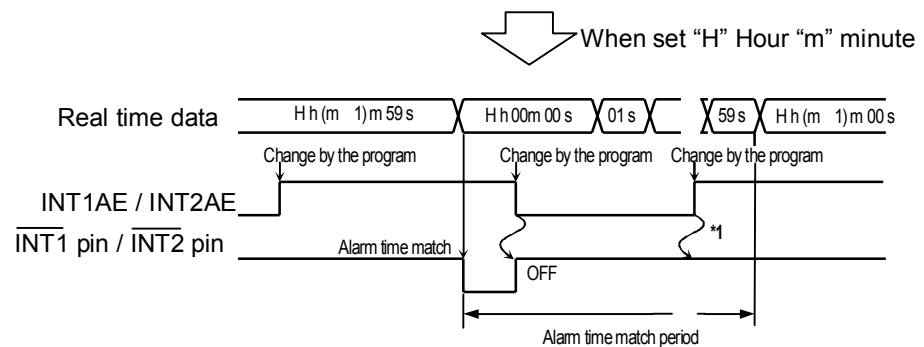
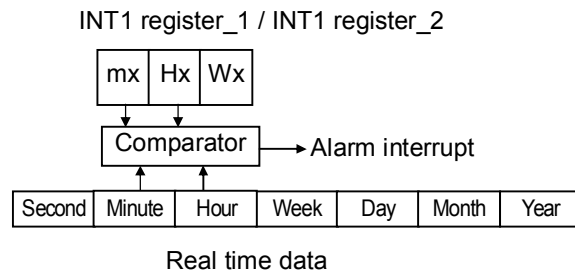
In case of AxWE = AxHE = AxmE = "1"

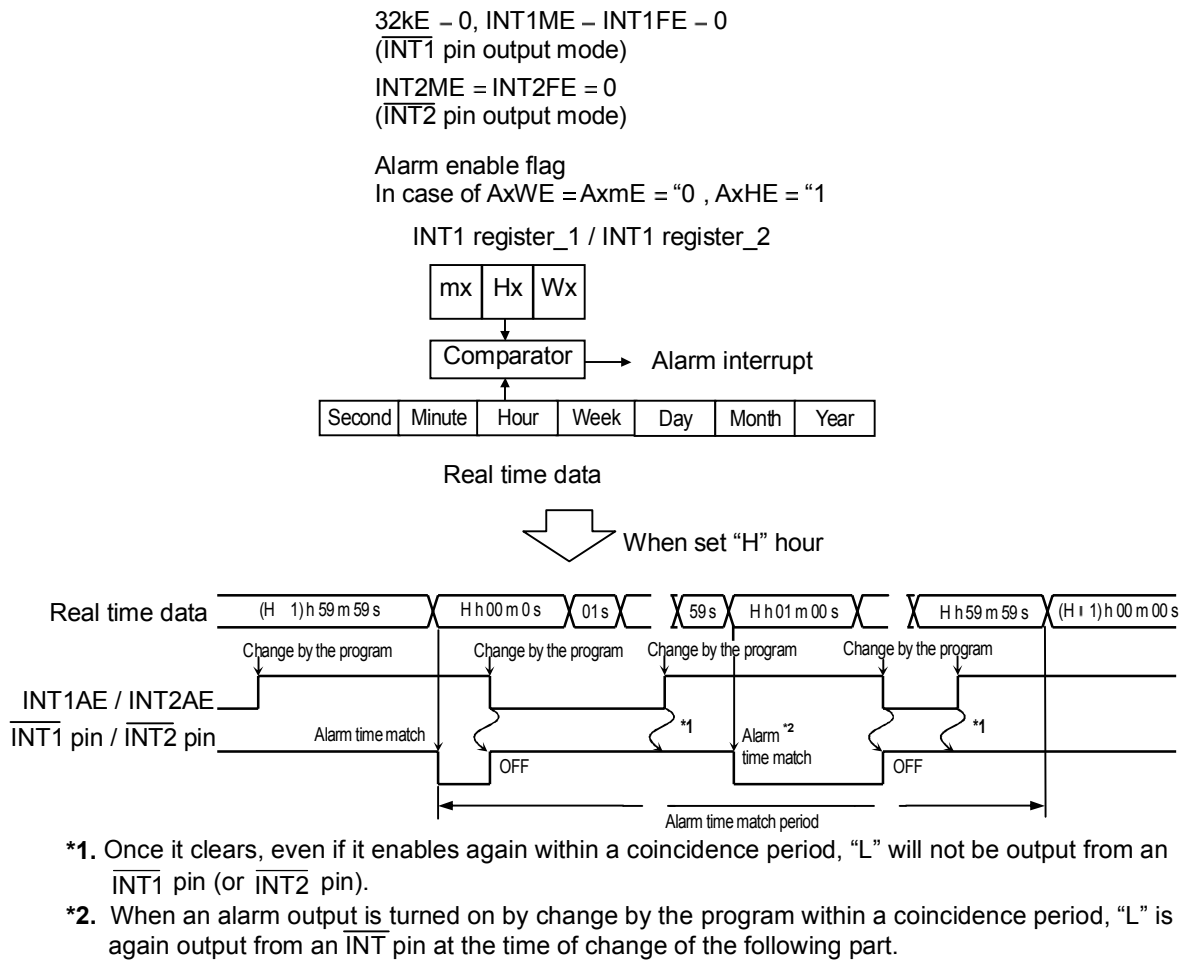


32kE = 0, INT1ME = INT1FE = 0  
( $\overline{\text{INT1}}$  pin output mode)  
INT2ME = INT2FE = 0  
( $\overline{\text{INT2}}$  pin output mode)

Alarm enable flag

In case of AxWE = "0", AxHE = AxmE = "1"



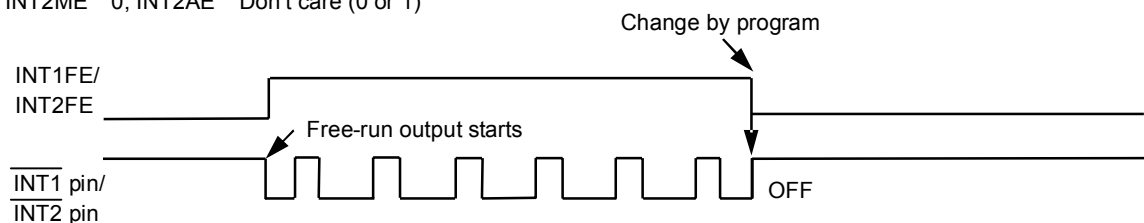


**Figure 17 Timing of Alarm Interrupt Output**

**(2) Selected frequency steady interrupt output**

When the INT1 (or INT2) pin output mode is set as the selected frequency steady interrupt setting using status register\_2 and the frequency/duty data is set in INT1 register\_1 (or INT1 register\_2), the set clock is output.

32kE = 0, INT1ME = 0, INT1AE Don't care (0 or 1)  
 INT2ME = 0, INT2AE Don't care (0 or 1)

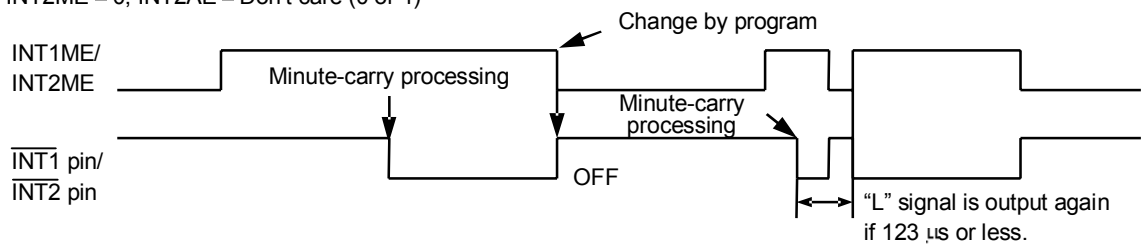


**Figure 18 Timing of Selected Frequency Steady Interrupt Output**

**(3) Per-minute edge interrupt output**

When the first minute carry is performed after the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin output mode is set as the per-minute edge interrupt using status register\_2, low is output from the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin. Since the output is held, in the  $\overline{\text{INT1}}$  pin output mode, rewrite 32kE, INT1AE, INT1ME, and INT1FE of status register\_2 to "0", and in the  $\overline{\text{INT2}}$  pin output mode, rewrite INT2AE, INT2ME, and INT2FE of status register\_2 to "0" using serial communication to set the output to high (OFF state).

32kE = 0, INT1ME = 0, INT1AE = Don't care (0 or 1)  
INT2ME = 0, INT2AE = Don't care (0 or 1)



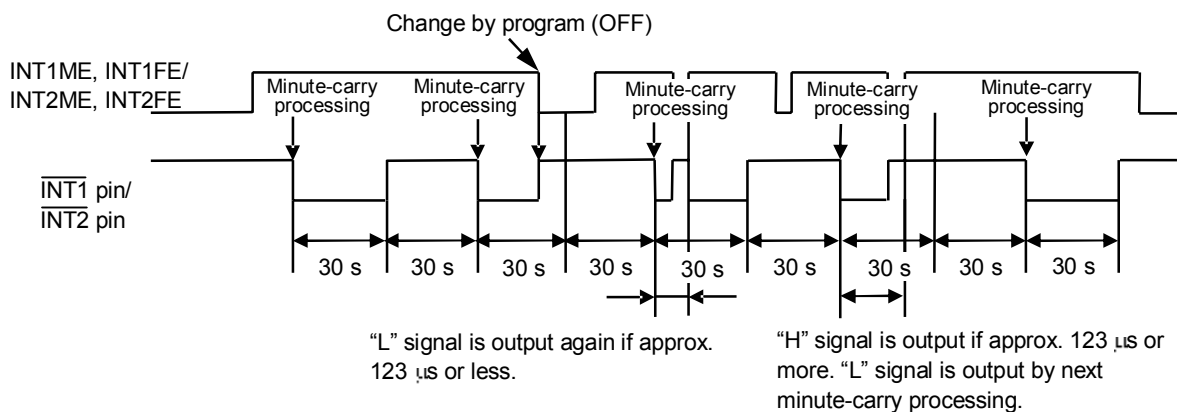
**Figure 19 Timing of Per-Minute Edge Interrupt Output**

**Caution** Since the minute carry processing signal is retained for 123  $\mu\text{s}$ , if communication disable or enable is executed during this period, low is output from the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin again.

**(4) Per-minute steady interrupt output 1**

When the first minute carry is performed after the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin output mode is set as per-minute steady interrupt 1 using status register\_2, a clock whose cycle is 1 minute (50% duty) is output from the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin.

32kE = 0, INT1AE = 0 ( $\overline{\text{INT1}}$  pin output mode)  
INT2AE = 0 ( $\overline{\text{INT2}}$  pin output mode)



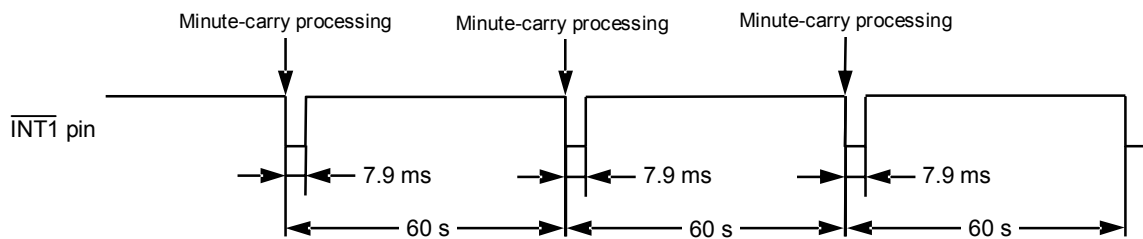
**Figure 20 Timing of Per-Minute Steady Interrupt Output 1**

**Caution** When communication disable or enable is executed while the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin is low, low is output from the  $\overline{\text{INT1}}$  (or  $\overline{\text{INT2}}$ ) pin again.

(5) Per-minute steady interrupt output 2 ( $\overline{\text{INT1}}$  pin output mode only)

When the first minute carry is performed after the  $\overline{\text{INT1}}$  pin output mode is set as per-minute steady interrupt 2 using status register\_2, low is output from the  $\overline{\text{INT1}}$  pin for a period of 7.9 ms in synchronization with the minute carry processing inside the IC. However, when real-time data is read, the minute carry processing is delayed by a maximum of 0.5 s and accordingly low output from the  $\overline{\text{INT1}}$  pin is also delayed by a maximum of 0.5 s. When the second data is rewritten by a real-time data write command, counting starts from the rewritten second data and as a result, the output interval during that period may become either longer or shorter.

(a) During normal operation



(b) During realtime data read

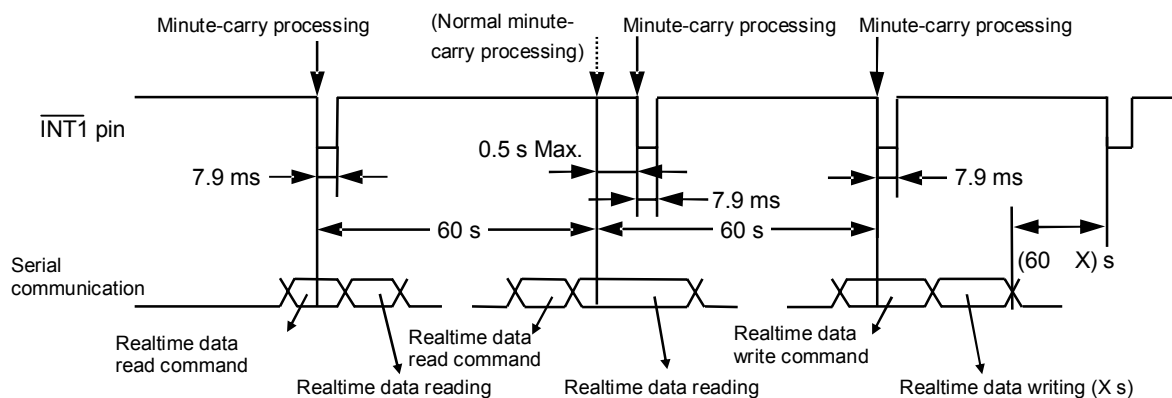
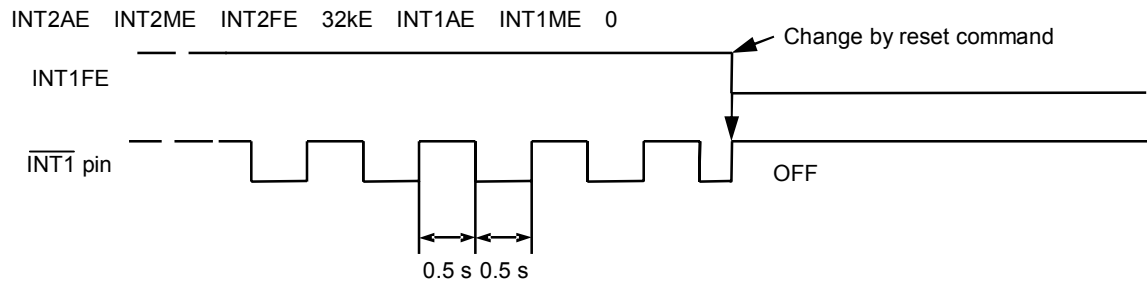


Figure 21 Timing of Per-Minute Steady Interrupt Output 2

- Caution**
1. When changing an output mode, give care to the state of INT1 register\_1 (or INT1 register\_2) and the output.
  2. If per-minute edge interrupt output or per-minute steady interrupt output is chosen, INT1 register\_1 (or INT1 register\_2) has no meaning.

**(6) During power-on detector operation**

When power is applied to this IC, power-on detection circuit operates, status register\_1 is set to "80h" (bit 7 (POC flag) of status register\_1 is set to 1) via the power-on detection circuit, and a 1 Hz clock is output from the  $\overline{\text{INT1}}$  pin.



**Figure 22  $\overline{\text{INT1}}$  Pin Output Timing During Power-on Detector Operation**

## ■ Clock Adjustment Function

A clock adjustment function is provided to logically perform slow/fast adjustment of the 32 kHz clock and correct a slow/fast clock with high accuracy. Use the clock adjustment register to set this function. When not using this function, be sure to set it to 00h.

The clock adjustment register value is calculated by the following expression.

### (1) If current oscillation frequency > target frequency (in case the clock is fast)

$$\text{Register value}^{*1} - 128 \quad \text{Integral value} \left( \frac{(\text{Current oscillation frequency actual measurement value}^{*2}) \quad (\text{Target oscillation frequency}^{*3})}{(\text{Current oscillation frequency actual measurement value}^{*2}) \times (\text{Minimum resolution}^{*4})} \right)$$

**Caution** The figure range which can be corrected is that the calculated value is from 0 to 64.

- \*1. The register value is the value set to the clock adjustment register. Set the binarized value of this value to the clock adjustment register.
- \*2. This is the measurement value of the signal that is output to the  $\overline{\text{INT1}}$  pin or  $\overline{\text{INT2}}$  pin when the 1 Hz clock output setting is:  
32kE = 0, INT1ME = 0, INT1FE = 1, INT1 register\_1 is 01h (for the  $\overline{\text{INT1}}$  pin)  
INT2ME = 0, INT2FE = 1, INT1 register\_2 is 01h (for the  $\overline{\text{INT2}}$  pin)
- \*3. This is the frequency to be adjusted by using the clock adjustment function.
- \*4. For the minimum resolution, 3.052 ppm or 1.017 ppm can be set using B7 of the clock adjustment register. When B7 is 0, 3.052 ppm is set and logical slow/fast adjustment is performed every 20 seconds. When B7 is 1, 1.017 ppm is set and logical slow/fast adjustment is performed every 60 seconds.

**Table 13**

	B7 = 0	B7 = 1
Slow/fast adjustment	Every 20 seconds	Every 60 seconds
Minimum resolution	3.052 ppm	1.017 ppm
Correction range	195.3 ppm to 192.2 ppm	65.1 ppm to 64.1 ppm

### ◆ The example of calculated value 1

Current oscillation frequency actual measurement value = 1.000080 [Hz],

Target oscillation frequency = 1.000000 [Hz],

B7 = 0 (minimum resolution = 3.052 ppm),

$$\text{Register value} - 128 \quad \text{Integral value} \left( \frac{(1.000080) \quad (1.000000)}{(1.000080) \times (3.052 \times 10^{-6})} \right)$$

$$= 128 \quad \text{Integral value} (26.21) = 128 \quad 26 = 102$$

Thus, set up (B7,B6,B5,B4,B3,B2,B1,B0) = (0,1,1,0,0,1,1,0) for the clock adjustment register.



**(2) If current oscillation frequency < target frequency (in case the clock is slow)**

$$\text{Register value} - \text{Integral value} \left\{ \frac{\left( \frac{\text{Target oscillation frequency}}{\text{Current oscillation frequency}} \times \frac{\text{Current oscillation frequency actual measurement value}}{\text{Minimum resolution}} \right) - 1}{1} \right\}$$

**Caution** The figure range which can be corrected is that the calculated value is from 0 to 62.

## ◆ The example of calculated value 2

Current oscillation frequency actual measurement value = 0.999920 [Hz],  
 Target oscillation frequency = 1.000000 [Hz],  
 B7 = 0 (minimum resolution = 3.052 ppm),

$$\text{Register value} - \text{Integral value} \left\{ \frac{\left( \frac{1.000000}{0.999920} \times \frac{0.999920}{3.052 \times 10^{-6}} \right) - 1}{1} \right\}$$

$$= \text{Integral value} (26.21) + 1 = 26 + 1 = 27$$

Thus, set up (B7,B6,B5,B4,B3,B2,B1,B0) = (0,0,0,1,1,0,1,1) for the clock register.

## ◆ The example of calculated value 3

Current oscillation frequency actual measurement value = 0.999920 [Hz],  
 Target oscillation frequency = 1.000000 [Hz],  
 B7 = 1 (minimum resolution = 1.017 ppm),

$$\text{Register value} - \text{Integral value} \left\{ \frac{\left( \frac{1.000000}{0.999920} \times \frac{0.999920}{1.017 \times 10^{-6}} \right) - 1}{1} \right\}$$

$$= \text{Integral value} (78.66) + 1$$

Thus, this calculated value exceeds the correctable range 0 to 62,  
 B7 = "1" (minimum resolution = 1.017 ppm) indicates the correction is impossible.

## ■ Serial Interface

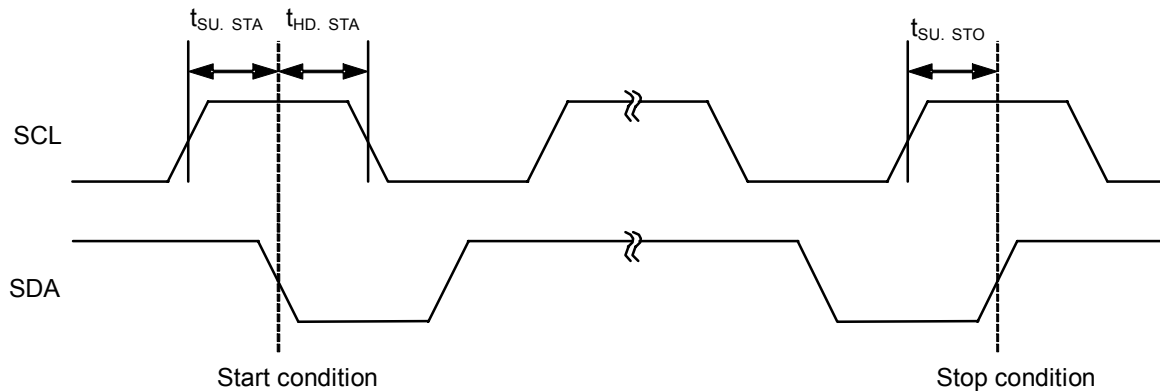
The S-35390A receives various commands via an I<sup>2</sup>C-BUS serial interface to read/write data. This section covers the transfer methods via I<sup>2</sup>C-BUS.

### 1. Start condition

The start condition is established at the point where the SDA line changes from “H” to “L” when the SCL line is “H” level. All operations start with the start condition.

### 2. Stop condition

The stop condition is established at the point where the SDA line changes from “L” to “H” when the SCL line is “H” level. If the stop condition is received during a readout sequence, the read operation is discontinued and the device enters the standby mode.

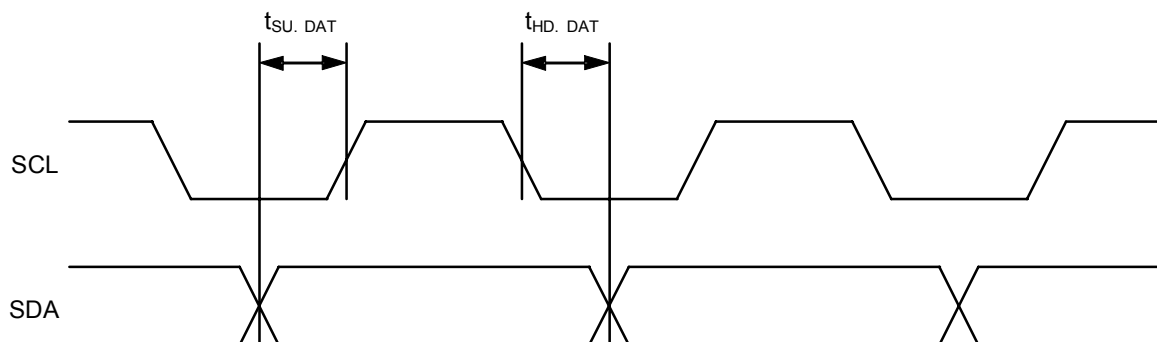


**Figure 23 Start Condition and Stop Condition**

### 3. Data transfer

Data transfer is performed by changing the SDA line during the period that the SCL line is “L”.

If the SDA line changes during the period that the SCL line is “H”, it is recognized as the start or stop condition.



**Figure 24 Timing of Data Transfer**

#### 4. Acknowledge

Data is transferred 8 bits in a row. Subsequently, in the 9th clock cycle period, the device on the system bus that is receiving the data changes the SDA line to “L” and returns the acknowledge signal to acknowledge data reception.

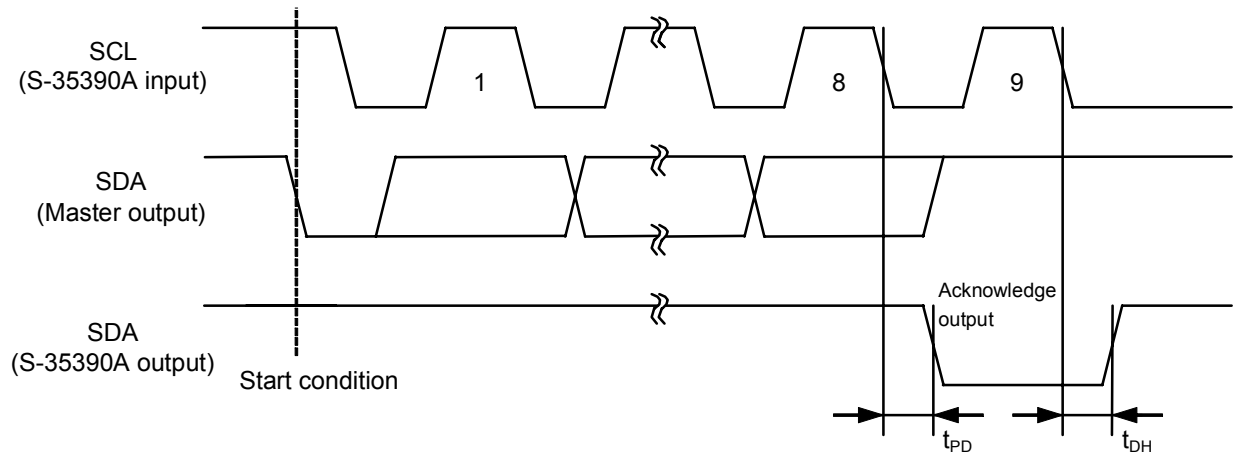


Figure 25 Timing of Acknowledge Output

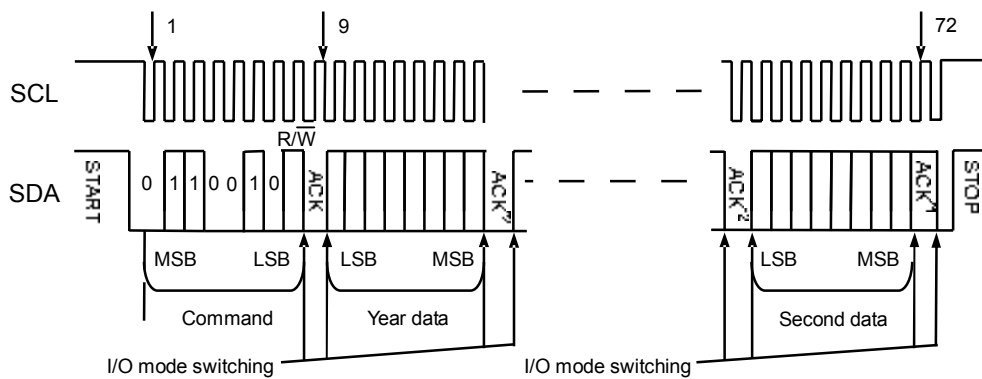
#### 5. Data reading

After detecting the start condition from outside, a device code and command are received. If the read/write bit is “1” at this point, the data read mode is entered. The data output sequence is output from the LSB.

## 6. Data writing

After detecting the start condition from outside, a device code and command are received. If the read/write bit is "0" at this point, the real-time data write mode or another register write mode is entered. Input the data input sequence for both the real-time data write mode and status register write mode from the LSB. In real-time data writing, the calendar and time counter is reset by the rising of the ACK signal after the real-time write command and update operations are then prohibited. Subsequently, when minute data reception is completed, an end-of-month correction is performed while the second data is loaded. Counting up is started from the rising of the ACK signal after the second data reception.

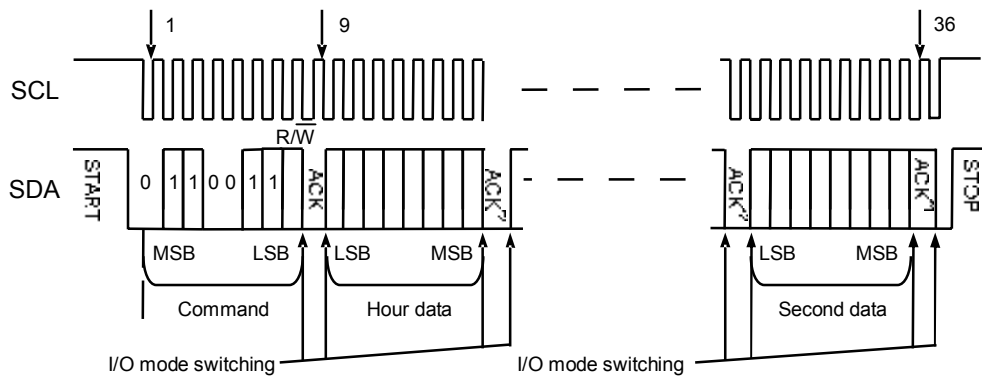
### (1) Real-time data access 1



- \*1. During reading, set NO\_ACK to 1.
- \*2. During reading, transmit ACK = 0 to S-35390A from the master device.

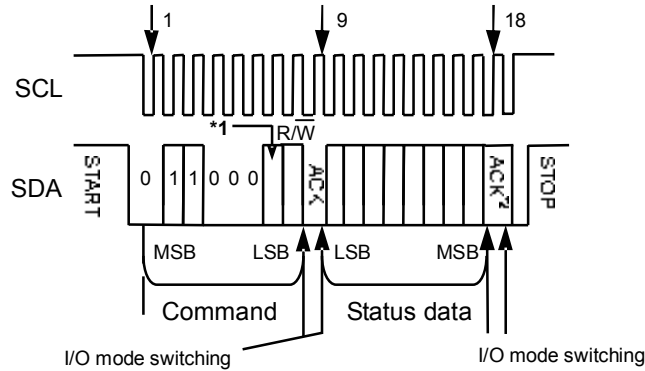
**Figure 26 Real-time Data Access 1**

### (2) Real-time data access 2



- \*1. During reading, set NO\_ACK to 1.
- \*2. During reading, transmit ACK = 0 to S-35390A from the master device.

**Figure 27 Real-time Data Access 2**

**(3) Status register\_1 access and status register\_2 access**

- \*1. 0: Status register\_1 selected, 1: Status register\_2 selected  
 \*2. During reading, set NO\_ACK to 1.

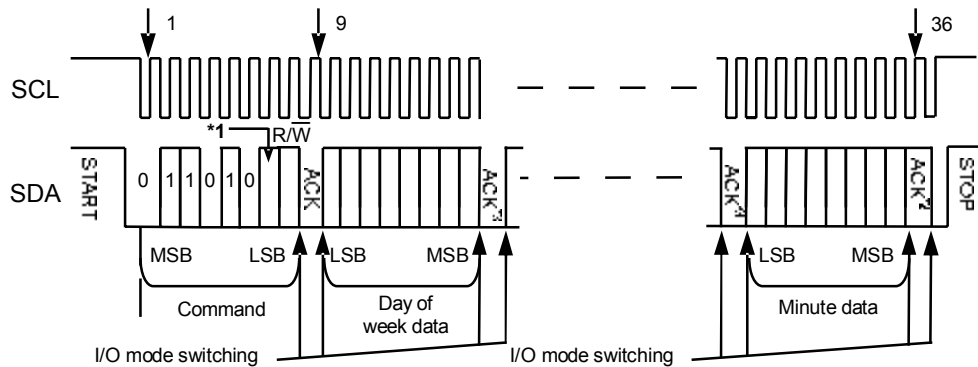
**Figure 28 Status Register\_1 Access and Status Register\_2 Access****(4) INT1 register\_1 access and INT1 register\_2 access**

Since data written to and read from INT1 register\_1 varies according to the setting of status register\_2, be sure to set status register\_2 before reading/writing INT1 register\_1. When an alarm is set using status register\_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers. When the selected frequency steady interrupt setting is set, the data in these registers is frequency duty setting data.

**Caution** Alarm data and frequency duty data cannot be operated simultaneously.

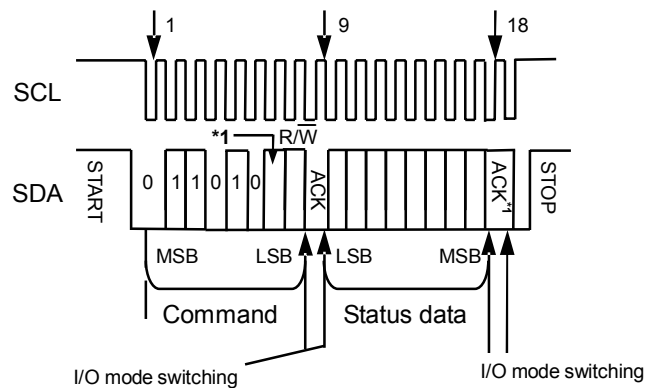
Since data written to and read from INT1 register\_2 varies according to the setting of status register\_2, be sure to set status register\_2 before reading/writing INT1 register\_1. When an alarm is set using status register\_2, these registers function as 3-byte alarm time data registers, and other than that, they function as 1-byte registers. When the selected frequency steady interrupt setting is set, the data in these registers is frequency duty setting data.

For details of each data, refer to “Status register\_1” and “Status register\_2”.



- \*1. 0: INT1 register\_1 selected, 1:INT1 register\_2 selected  
 \*2. During reading, set NO\_ACK to 1.  
 \*3. During reading, transmit ACK = 0 to S-35390A from the master device.

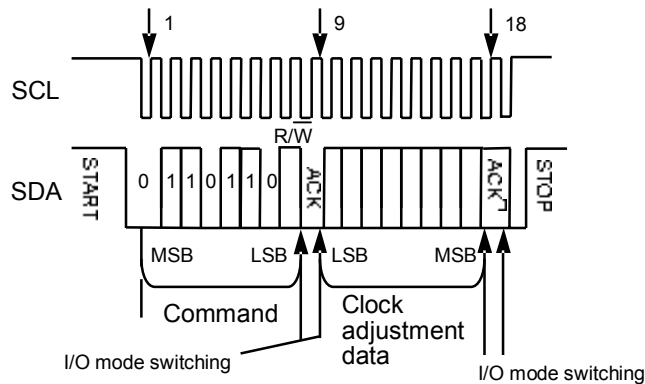
**Figure 29 INT1 Register\_1 Access and INT1 Register\_2 Access**



- \*1. 0: INT1 register\_1 selected, 1:INT1 register\_2 selected
- \*2. During reading, set NO\_ACK to 1.

**Figure 30 INT1 Register\_1 and INT1 Register\_2 (Frequency Duty Data) Access**

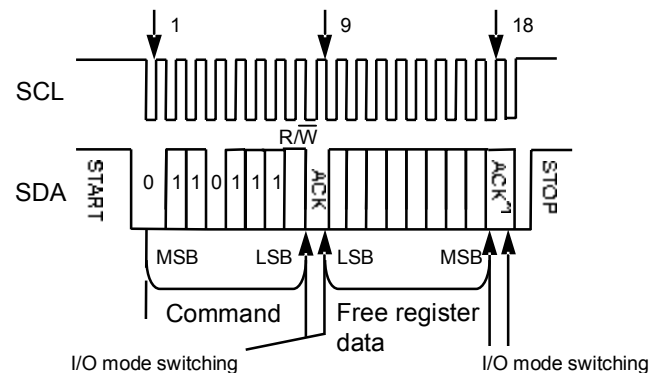
**(5) Clock adjustment register access**



- \*1. During reading, set NO\_ACK to 1.

**Figure 31 Clock Adjustment Register Access**

**(6) Free register access**

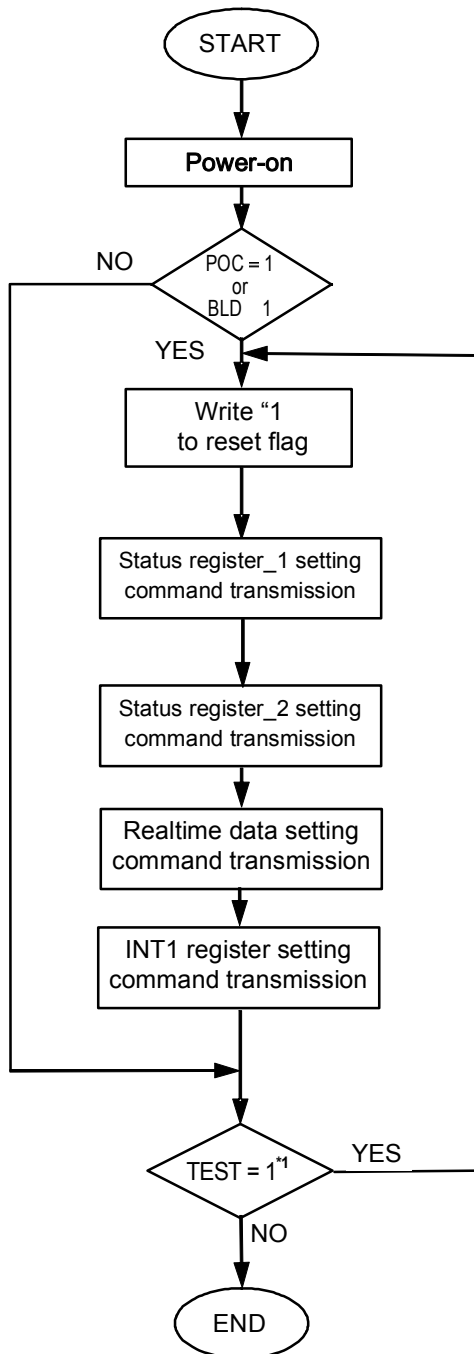


- \*1. During reading, set NO\_ACK to 1.

**Figure 32 Free Register Access**

## ■ Example of Software Processing

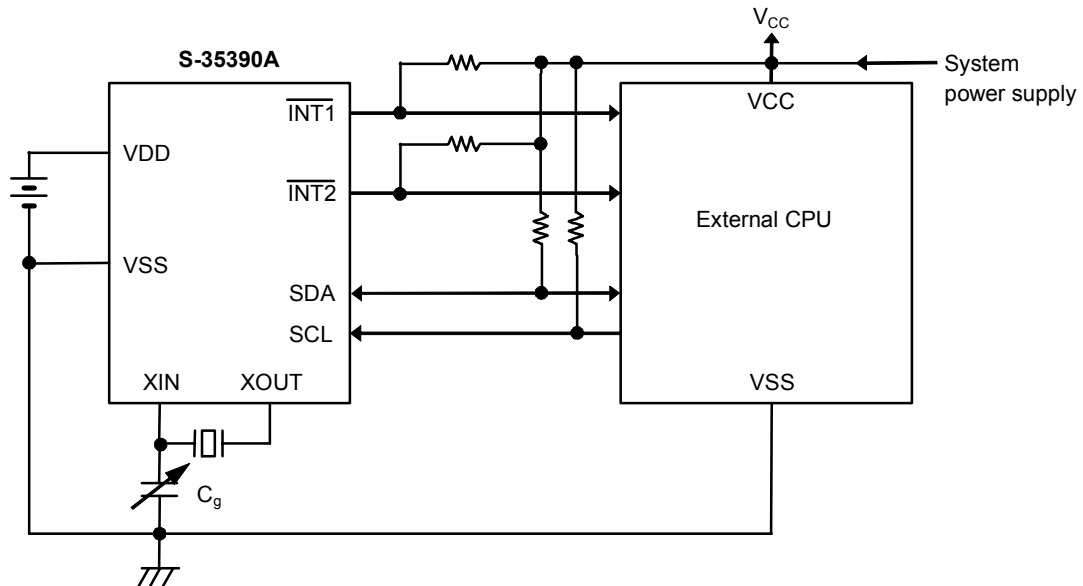
### 1. Initialization flow at power-on



\*1. If conditions are poor (e.g., in a noisy environment) and there is a high probability that commands transmitted via serial communication will be garbled, it is recommended to verify the TEST flag.

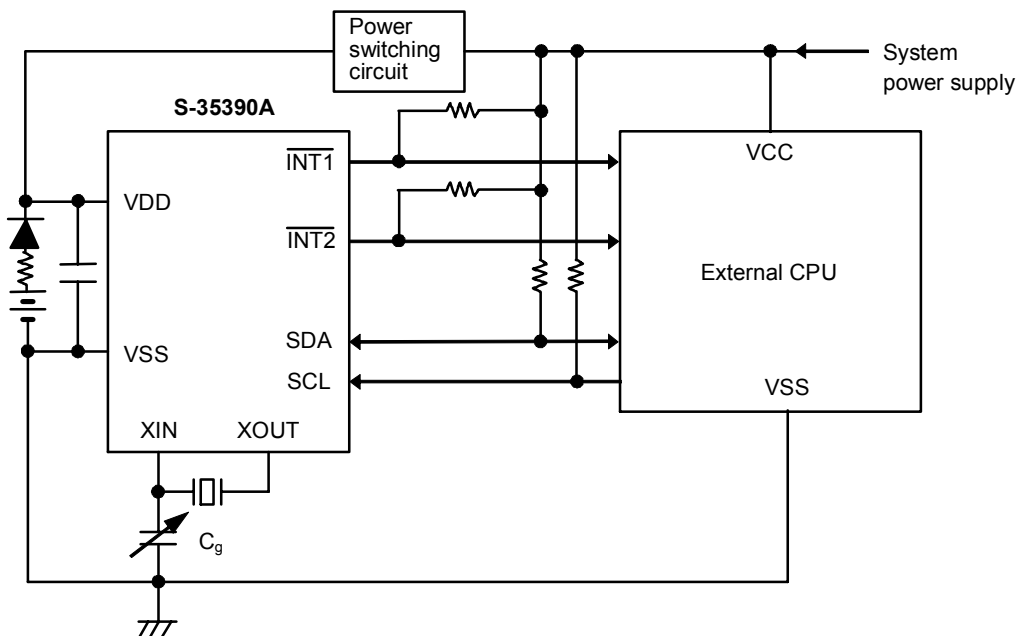
Figure 33 Initialization Flow

## ■ Examples of Application Circuits



- Caution**
1. Because the I/O pin has no protective diode on the VDD side, the relation of  $V_{CC} \geq V_{DD}$  is possible. But pay careful attention to the specifications.
  2. Communication should be executed after the system power supply is turned on and a stable state is obtained.

Figure 34 Application Circuit 1



- Caution** Communication should be executed after the system power supply is turned on and a stable state is obtained.

Figure 35 Application Circuit 2

- Caution** The above connection diagrams do not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

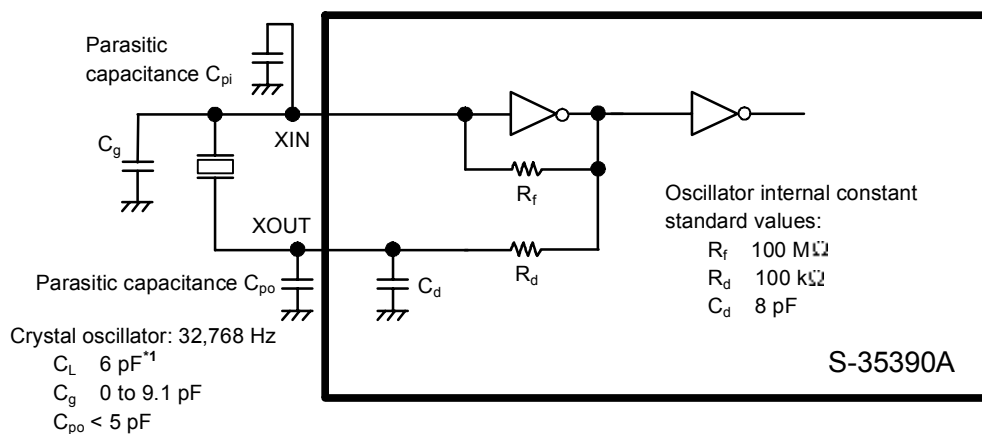


## ■ Adjustment of Oscillation Frequency

### 1. Configuration of oscillator

Since crystal oscillation is sensitive to external noise (the clock accuracy is affected), the following measures are essential for optimizing the oscillator configuration.

- (1) Place the S-35390A, crystal oscillator, and external capacitor ( $C_g$ ) as close to each other as possible.
- (2) Increase the insulation resistance between pins and the substrate wiring patterns of XIN and XOUT.
- (3) Do not place any signal or power lines close to the oscillator.



\*1. When using the crystal oscillator with a  $C_L$  value of 7 pF, externally connect  $C_d$ .

Figure 36 Connection Diagram 1

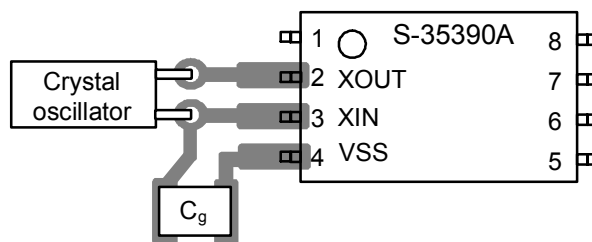


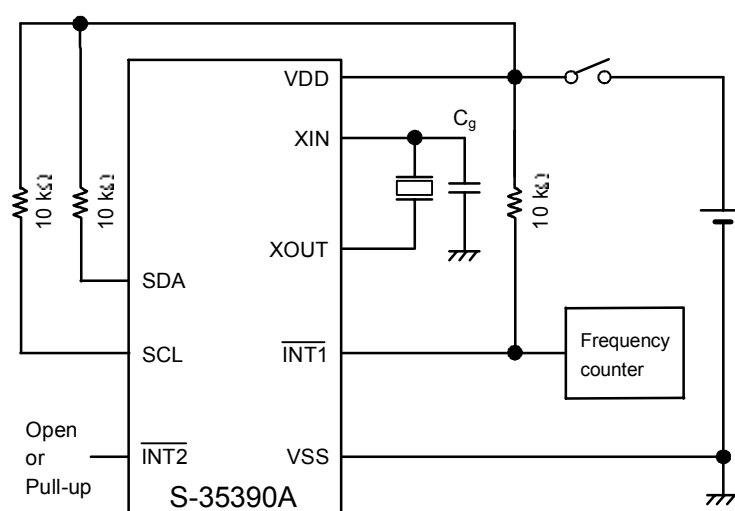
Figure 37 Connection Diagram 2

## 2. Measurement of oscillation frequency

When the S-35390A is turned on, the internal power-on detector operates and a signal of 1 Hz is output from the  $\overline{\text{INT1}}$  pin to select the crystal oscillator and optimize the  $C_g$  value. Turn the power on and measure the signal with a frequency counter following the circuit configuration shown in **Figure 38**. A signal of 1 Hz may not be output depending on the state in which power is applied, so set the selected frequency steady interrupt using status register\_2 and then set 1 Hz signal output using INT1 register\_1 to generate a normal output. For further details, refer to “**Interrupts**”.

**Remark** If the error range is  $-1$  ppm in relation to 1 Hz, the time is shifted by approximately 2.6 seconds per month (calculated using the following expression).

$$10^{-6} (1 \text{ ppm}) \times 60 \text{ seconds} \times 60 \text{ minutes} \times 24 \text{ hours} \times 30 \text{ days} = 2.592 \text{ seconds}$$



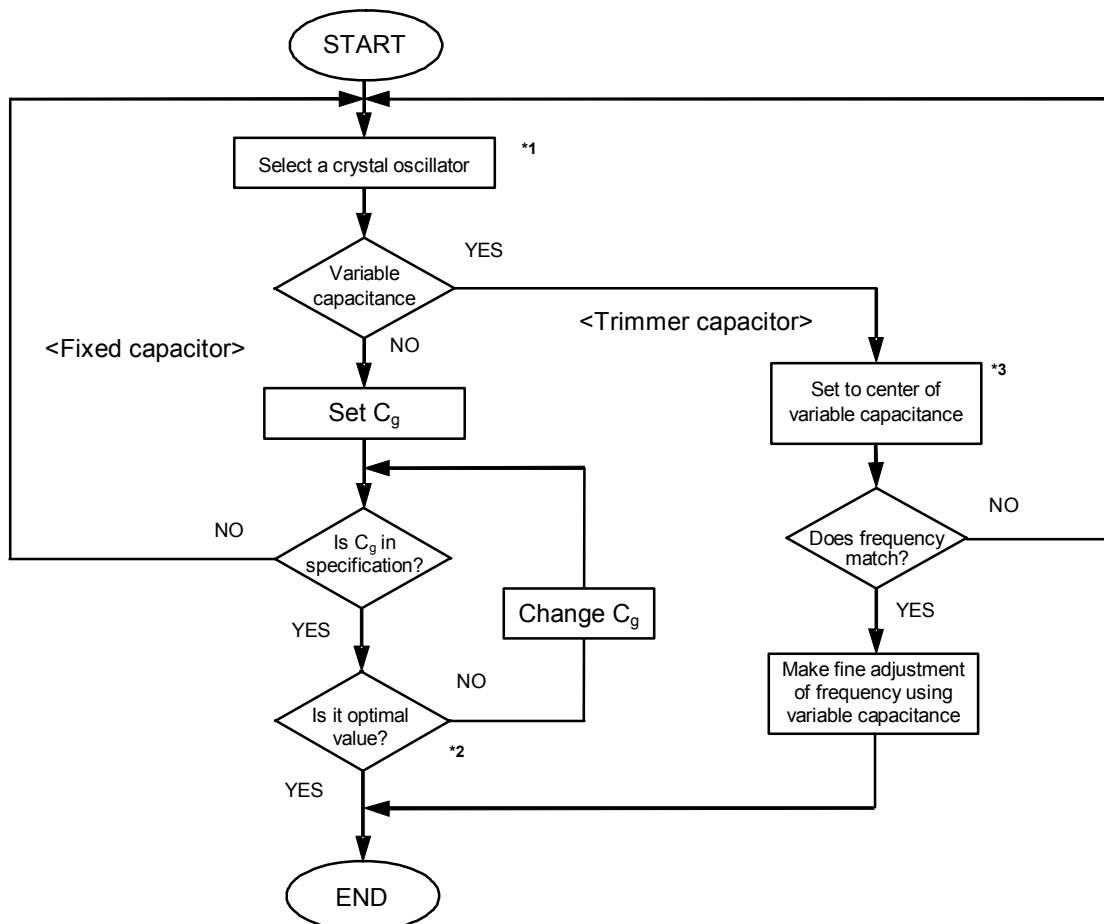
**Figure 38 Configuration of Oscillation Frequency Measurement Circuit**

- Caution**
1. Use a high-accuracy frequency counter (1 ppm order).
  2. Since the 1 Hz signal continues to be output, initialization must be executed during normal operation.
  3. Refer to the frequency slow/fast range characteristics for  $C_g$ .

### 3. Adjustment of oscillation frequency

#### (1) Adjustment by setting $C_g$

Matching of the crystal oscillator with the nominal frequency must be performed with the stray capacitance on the board included. Select a crystal oscillator and optimize the  $C_g$  value in accordance with the flowchart below.



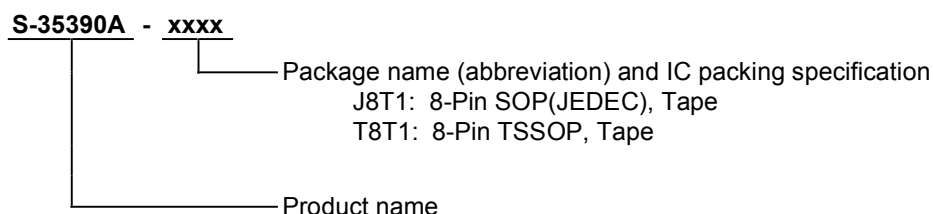
- \*1. For the matching adjustment of the IC with a crystal, contact the crystal manufacturer to determine the  $C_L$  value (load capacitance) and  $R_1$  value (equivalent series resistance).  $C_L = 6$  pF and  $R_1 = 30$  k $\Omega$  typ. are recommended values.
- \*2. The  $C_g$  value must be selected on the actual PCB since it is affected by stray capacitance. Select the external  $C_g$  value in a range of 0 pF to 9.1 pF.
- \*3. Adjust the rotation angle of the variable capacitance so that the capacitance value is slightly smaller than the center, and confirm the oscillation frequency and the center value of the variable capacitance. This is done in order to make the capacitance of the center value smaller than one half of the actual capacitance value because a smaller capacitance value increases the frequency variation.

Figure 39 Crystal Oscillator Setting Flow

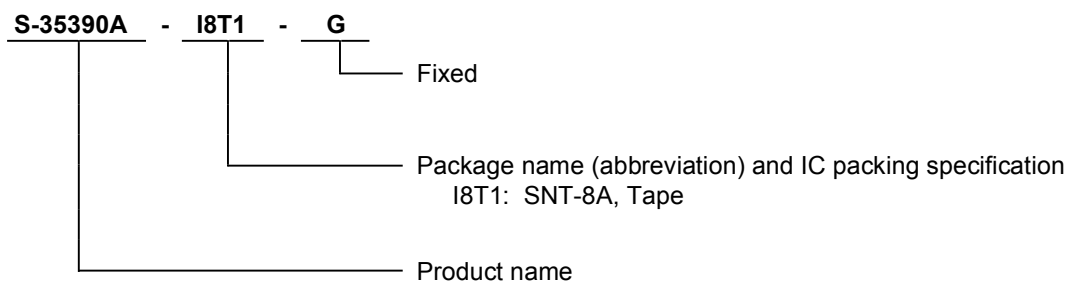
- Caution**
1. The oscillation frequency varies depending on the ambient temperature and power supply voltage. Refer to the characteristics examples.
  2. The 32 kHz crystal oscillator operates more slowly at an operating temperature than higher or lower 20 to 25°C. Therefore, it is recommended to adjust or set the oscillator to operate slightly faster at normal temperature.

## ■ Product Name Structure

### 1. 8-Pin SOP(JEDEC), 8-Pin TSSOP package



### 2. SNT-8A package



## ■ Precautions

- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
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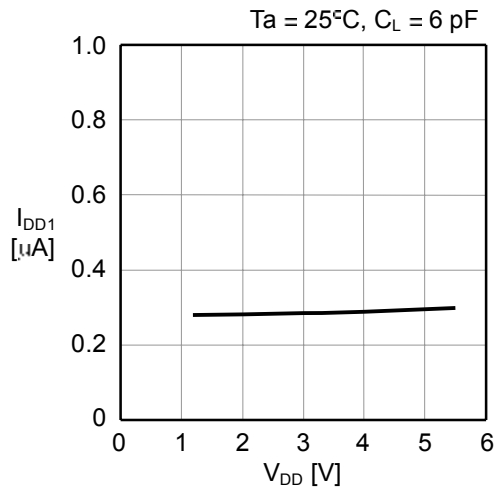
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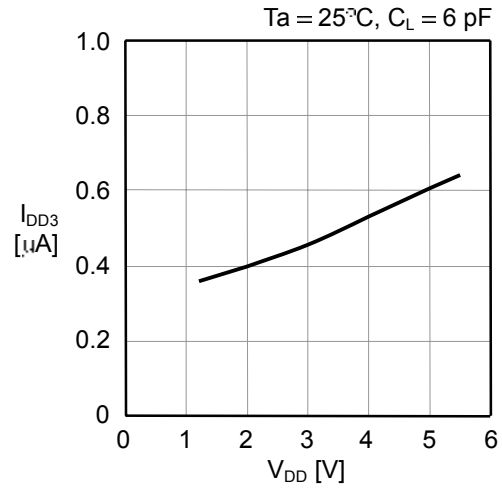
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## ■ Characteristics (Reference Values)

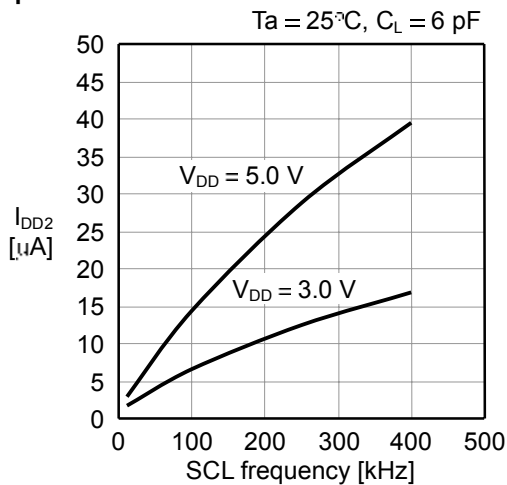
### (1) Standby current vs. $V_{DD}$ characteristics



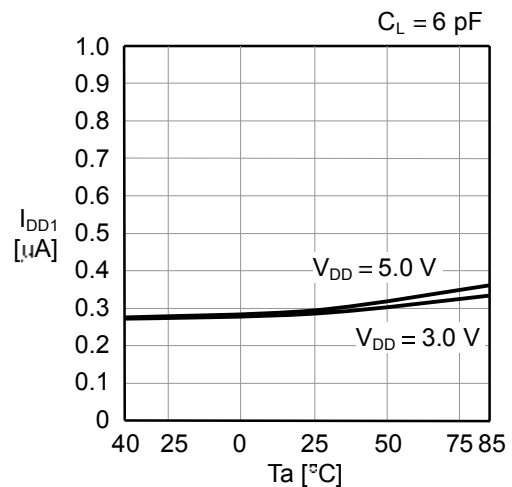
### (2) Current consumption during 32 kHz output vs. $V_{DD}$ characteristics



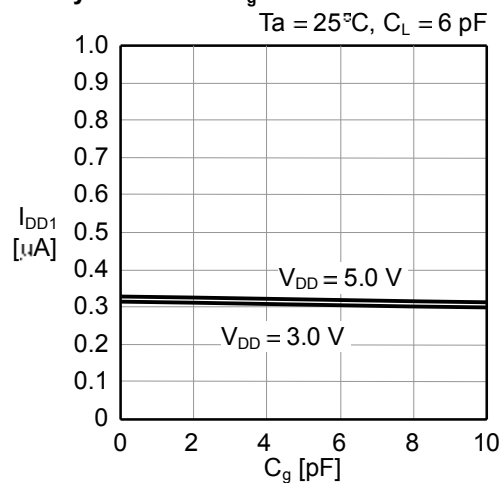
### (3) Current consumption during operation vs. Input clock characteristics



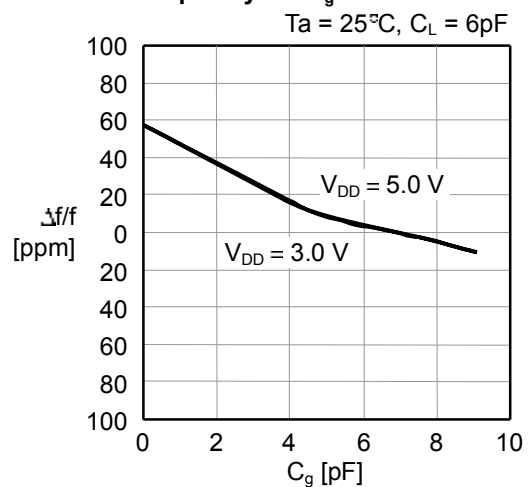
### (4) Standby current vs. Temperature characteristics



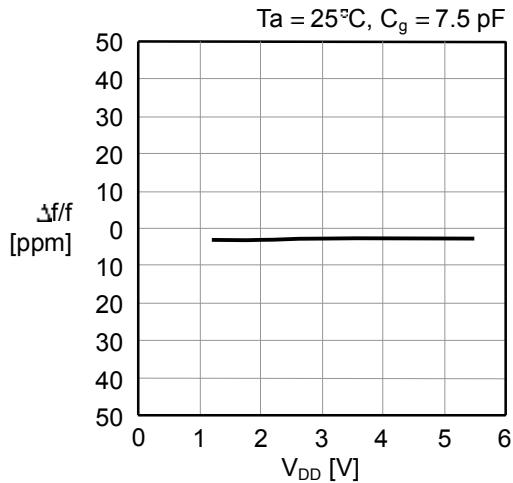
### (5) Standby current vs. $C_g$ characteristics



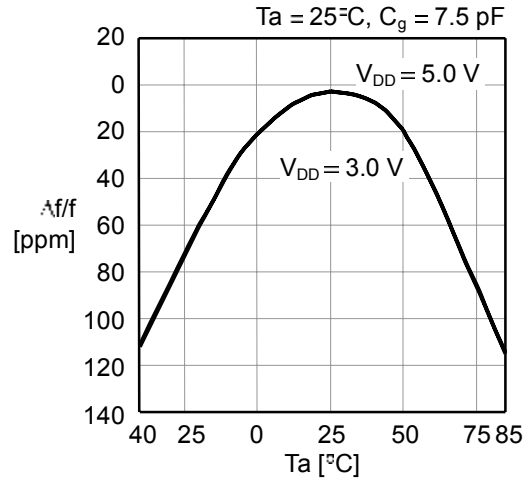
### (6) Oscillation frequency vs. $C_g$ characteristics



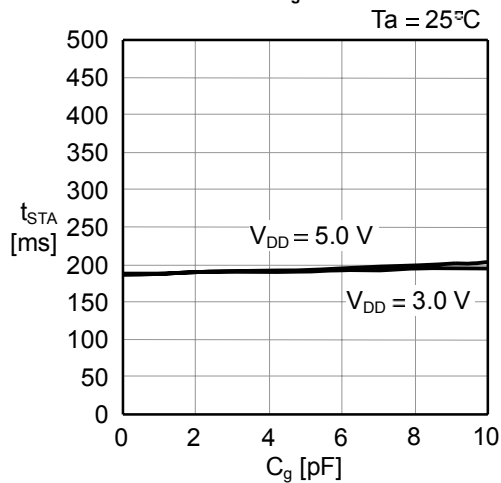
**(7) Oscillation frequency vs.  $V_{DD}$  characteristics**



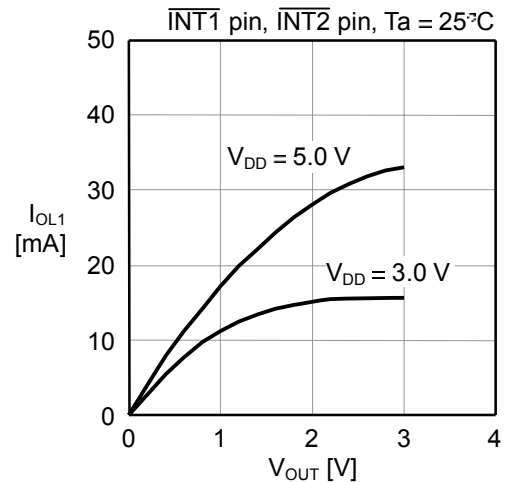
**(8) Oscillation frequency vs. Temperature characteristics**



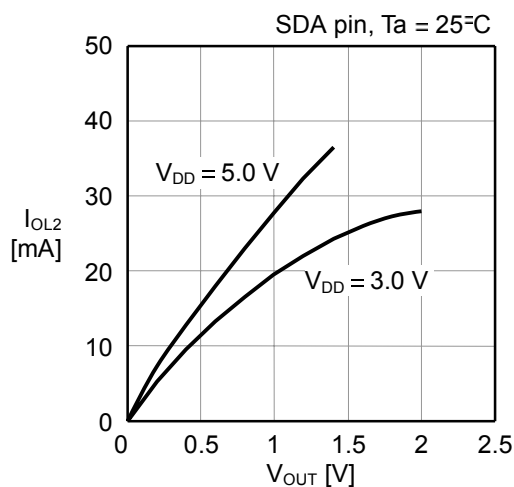
**(9) Oscillation start time vs.  $C_g$  characteristics**



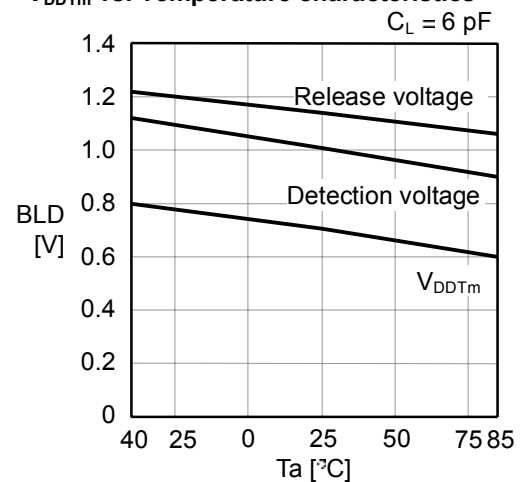
**(10) Output current characteristics 1 ( $V_{OUT}$  vs.  $I_{OL1}$ )**

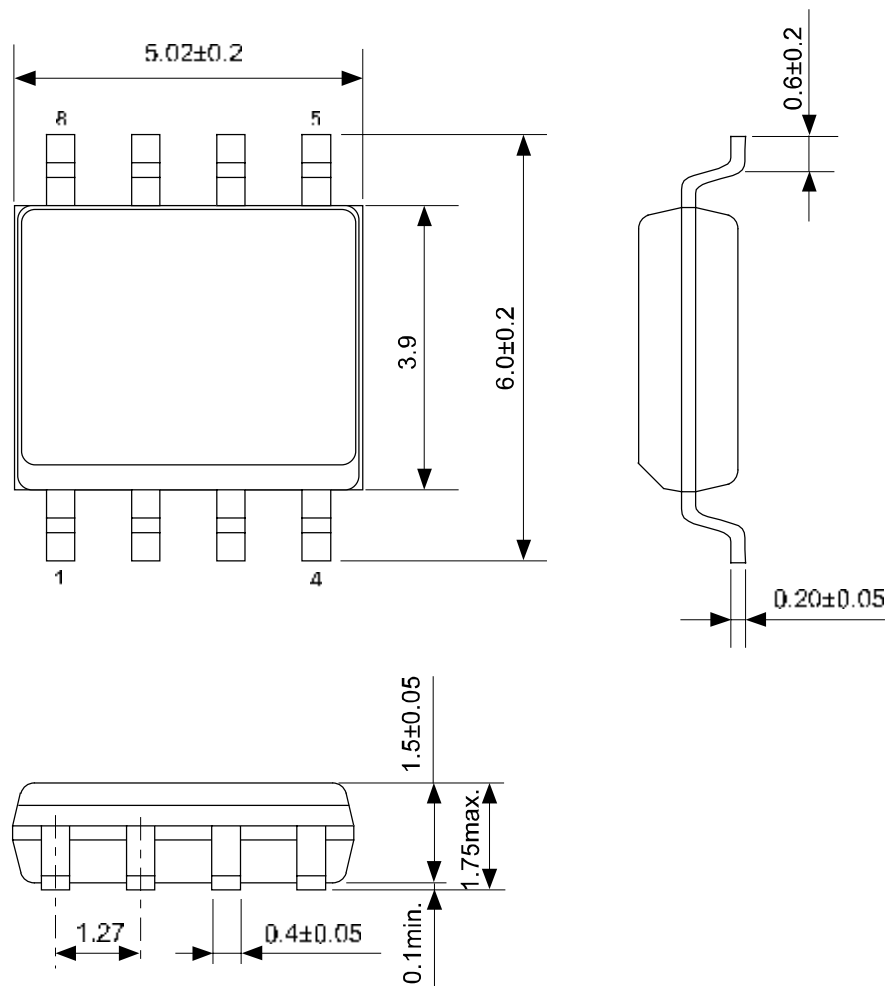


**(11) Output current characteristics 2 ( $V_{OUT}$  vs.  $I_{OL2}$ )**



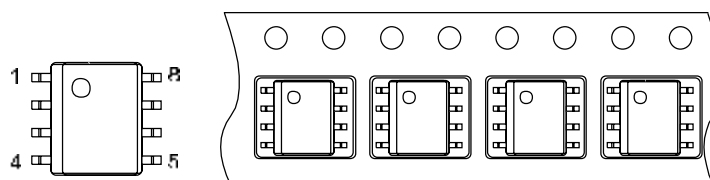
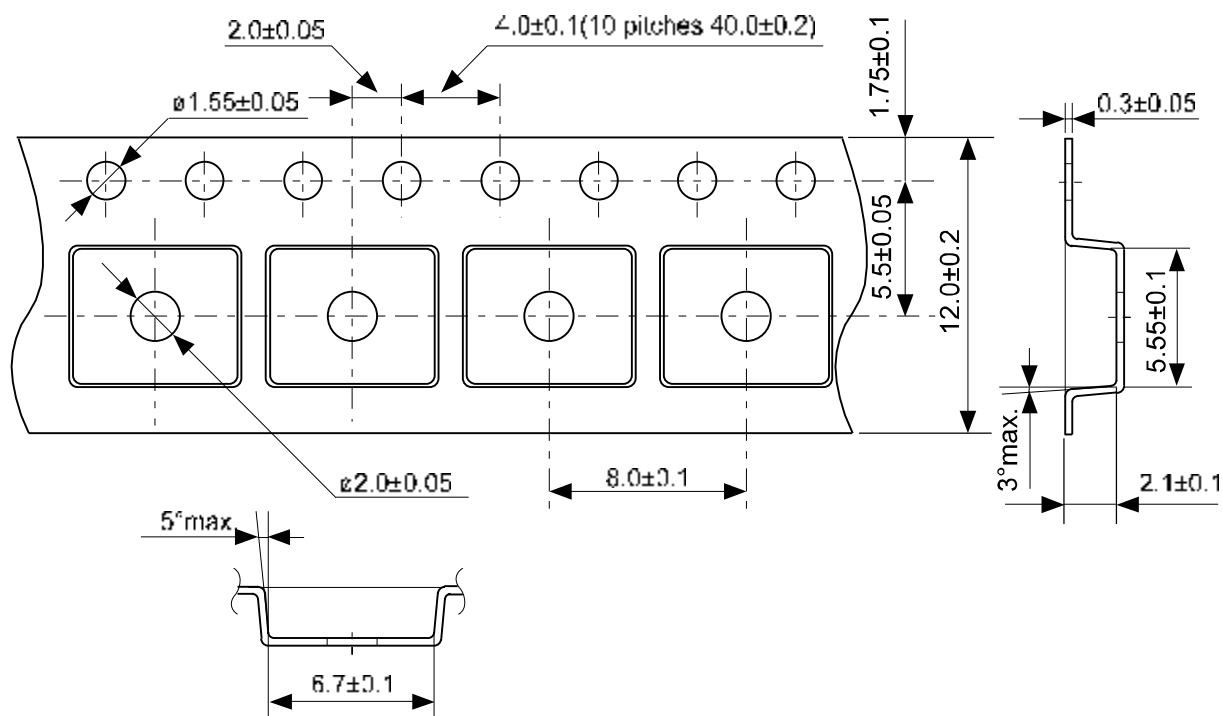
**(12) BLD detection, release voltage,  $V_{DDTm}$  vs. Temperature characteristics**





No. FJ008-A-P-SD-2.1

TITLE	SOP8J-D-PKG Dimensions
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

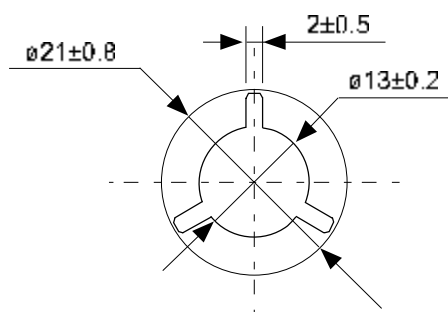
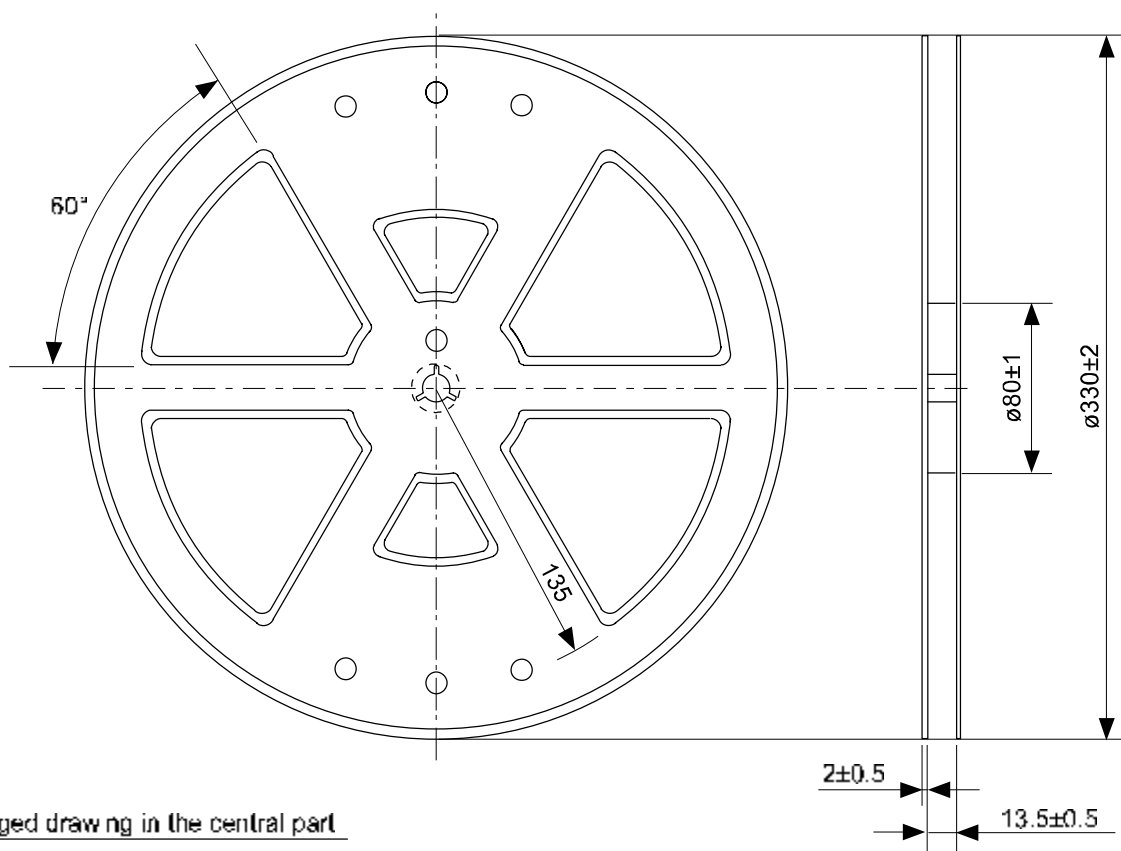


Feed direction

No. FJ008-D-C-SD-1.1

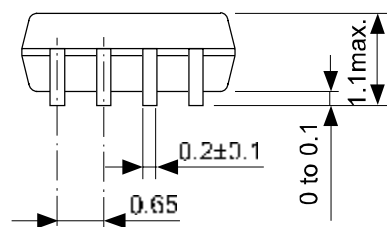
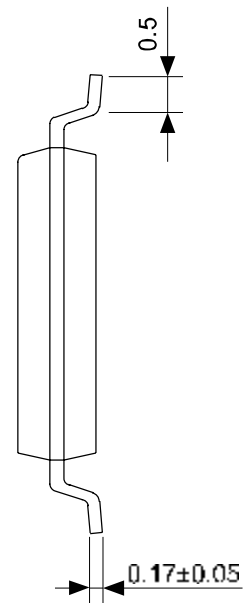
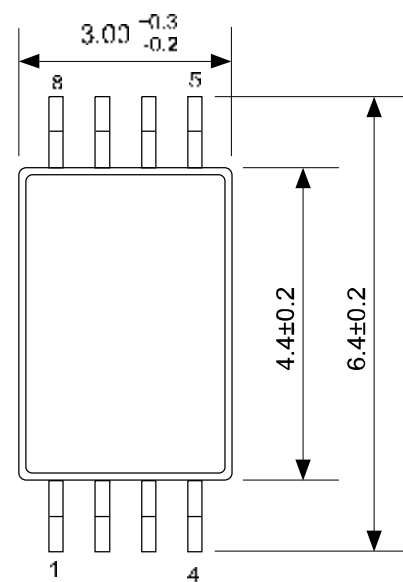
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No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	





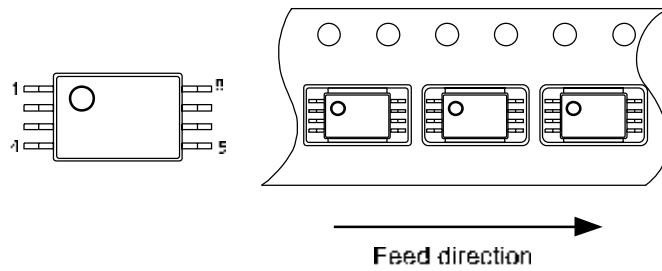
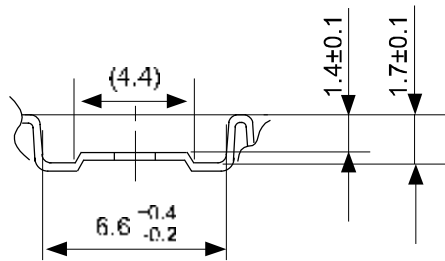
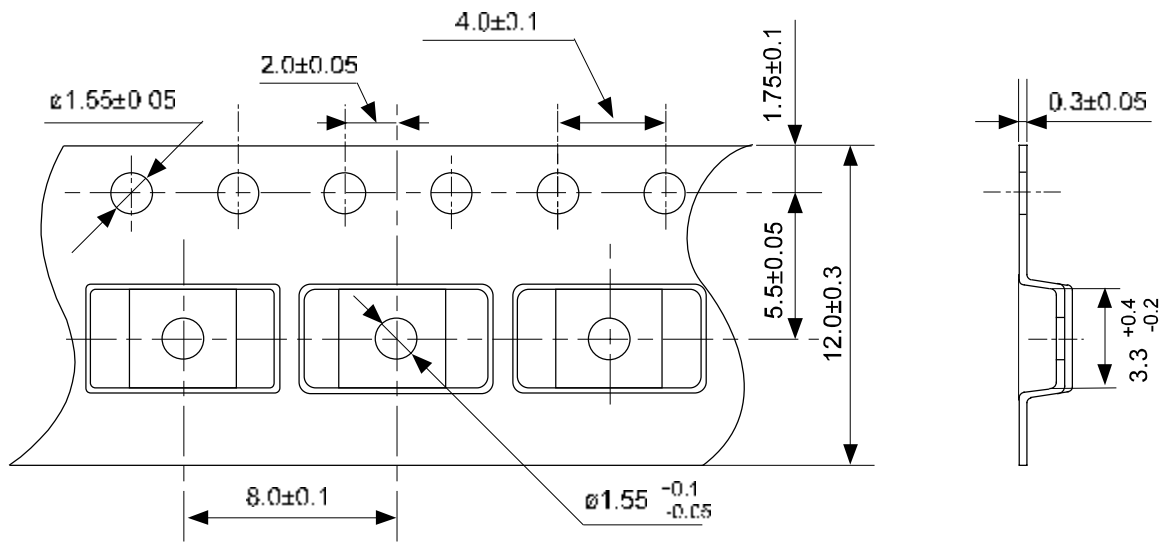
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UNIT	mm		
Seiko Instruments Inc.			



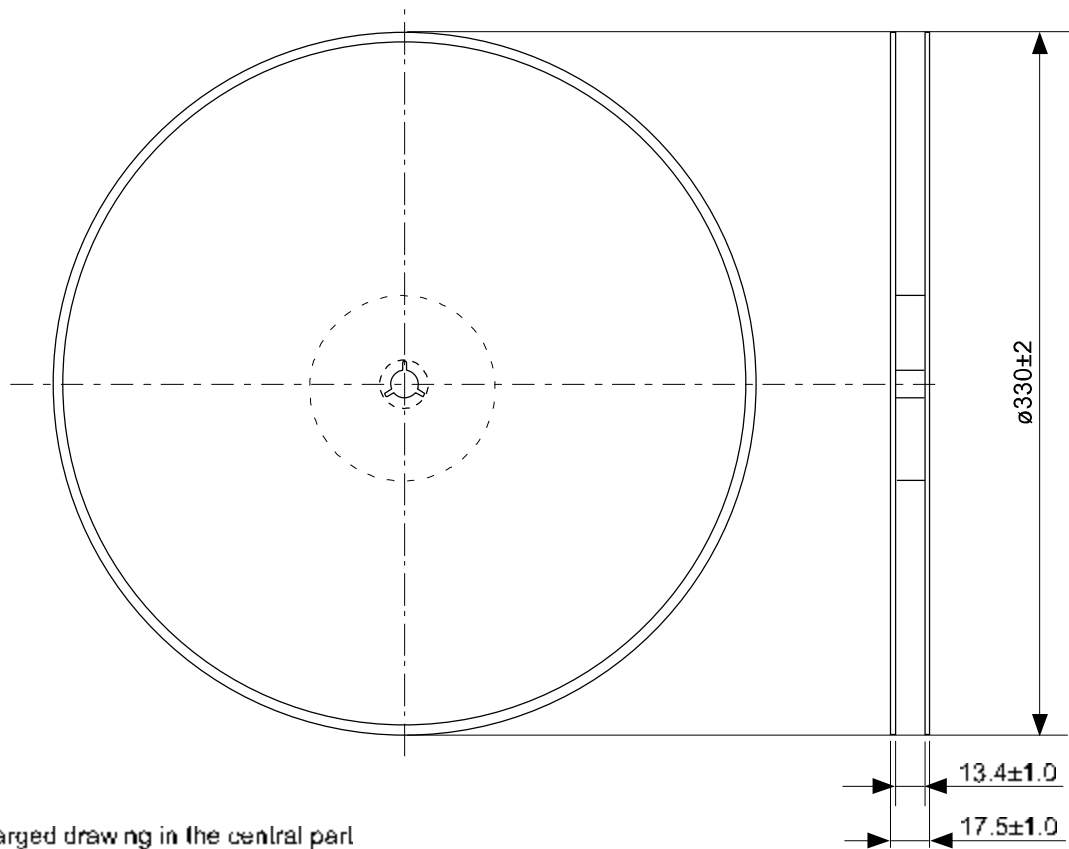
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
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UNIT	mm
Seiko Instruments Inc.	

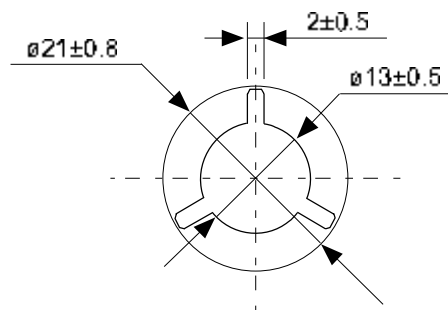


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
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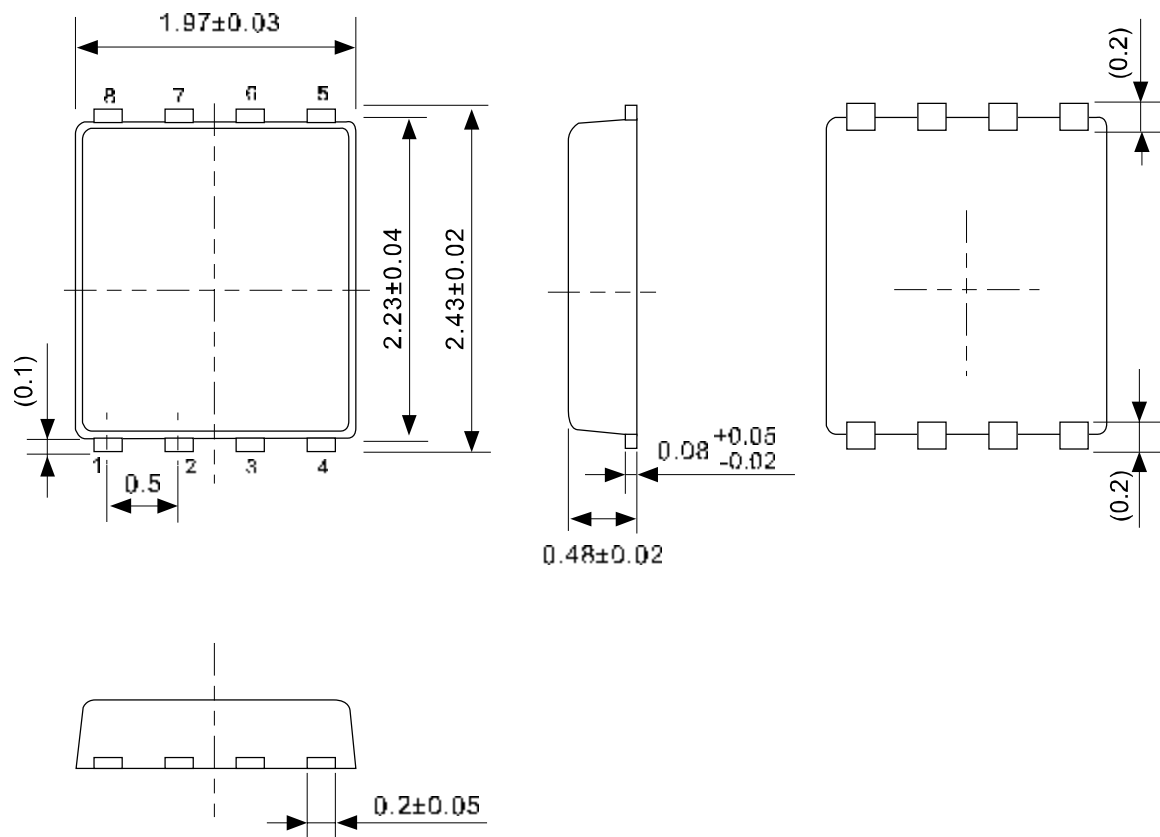


Enlarged drawing in the central part



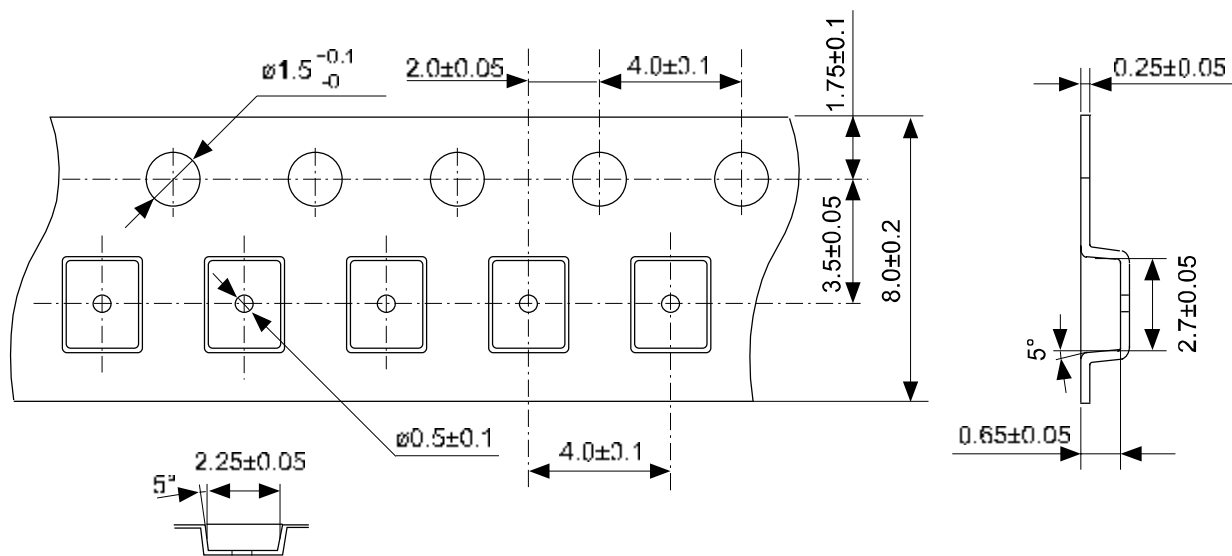
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Seiko Instruments Inc.			

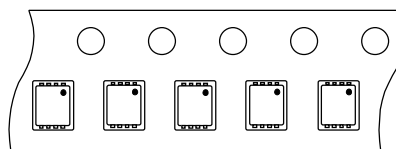


No. PH008-A-P-SD-1.0

TITLE	SNT-8A-A-PKG Dimensions
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SCALE	
UNIT	mm
Seiko Instruments Inc.	



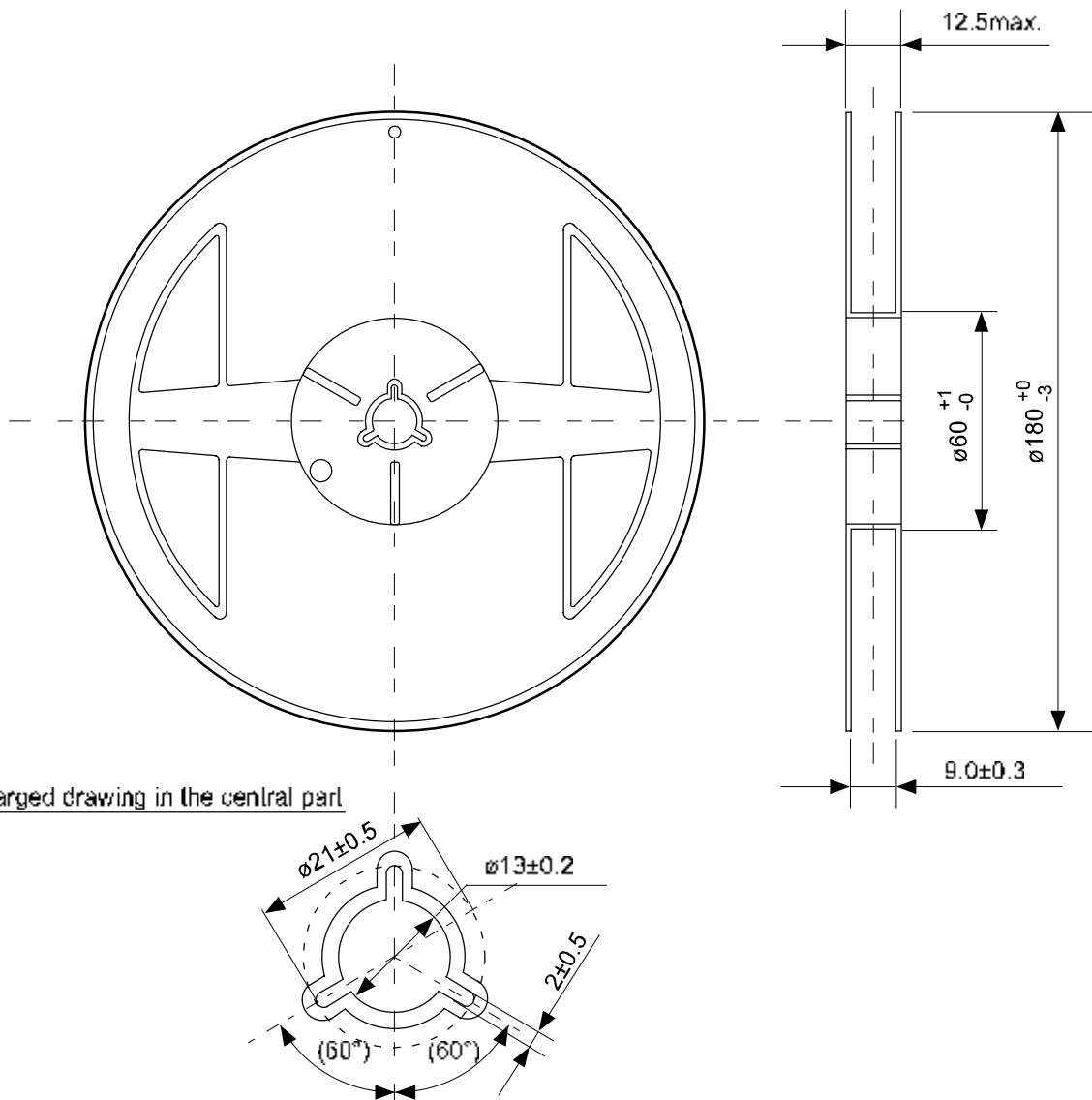
1321  
5578



Feed direction

No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part

No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5.000
UNIT	mm		
Seiko Instruments Inc.			

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## Test Report

No. F690101/LF-CTS015084

Date : April 23, 2004

Page 1 of 2

SEIKO INSTRUMENTS INC.

563, Takatsuka-Shinden, Matsudo-shi, Chiba 270-2222, Japan

The following merchandise was submitted and identified by the client as : -

Type of Product : TSSOP8-TG

SGS File No. : G-49/2004-2270/16

Country of Origin : Japan

Sample Receiving Date : Apr. 16, 2004

Test Performing Date : Apr. 19, 2004

Test Performed : SGS Testing Korea tested the sample which was selected by applicant with following result.

Test Results : For further details, please refer to following page.

SGS Testing Korea Co., Ltd.



Jason Han / Lab. Manager

KHJ/ykj

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## Test Report

No. F690101/LF-CTS015084

Date : April 23, 2004

Page 2 of 2

### Heavy Metal Test

Items	Unit	Test Method	DL	Results
Cadmium (Cd)	mg/kg	USEPA 3050B, ICP-AES	0.5	n. d.
Lead (Pb)	mg/kg	USEPA 3050B, ICP-AES	5	17
Mercury (Hg)	mg/kg	USEPA 3052, ICP-AES	0.5	n. d.
Hexavalent Chromium (Cr VI)	mg/kg	USEPA 3060A	0.16	n. d.

### Flame Retardants

Items	Unit	Test Method	D.L.	Results
<b>Polybrominated Biphenyls (PBBs)</b>	-	-	-	-
Bromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Dibromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Tribromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Tetrabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Pentabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Hexabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Heptabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Octabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
Decabromobiphenyl	mg/kg	SGS In-House Method	5	n. d.
<b>Polybrominated Diphenyl ethers (PBDEs)</b>	-	-	-	-
Bromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Dibromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Tribromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Tetrabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Pentabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Hexabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Heptabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Octabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.
Decabromodiphenyl ether	mg/kg	SGS In-House Method	5	n. d.

Note (1) n. d. = Not detected  
(2) D. L = Detection Limit

\*\*\*\*\* End \*\*\*\*\*

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